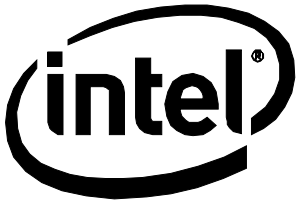


# Intel® Next Unit of Computing Board DCP847SKE

## Technical Product Specification

*January 2013*

*Order Number: G81548-002*

The Intel Next Unit of Computing Board DCP847SKE may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in the Intel Next Unit of Computing Board DCP847SKE Specification Update.

# Revision History

| Revision | Revision History | Date |
|---|---|---|
| 001 | First release of the Intel® Next Unit of Computing Board DCP847SKE Technical Product Specification | January 2013 |
| 002 | Specification clarification | January 2013 |

This product specification applies to only the standard Intel® Next Unit of Computing Board with BIOS identifier GKPPT10H.86A.

# Board Identification Information

**Basic Intel® Next Unit of Computing Board DCP847SKE Identification Information**

| AA Revision | BIOS Revision | Notes |
|---|---|---|
| G79416-101 | GKPPT10H.86A.0026 | 1,2 |
| G79416-104 | GKPPT10H.86A.0036 | 1,2 |

Notes:

1. The AA number is found on a small label on the component side of the board.
2. The Intel® QS77 PCH and Intel® Celeron® processor 847 used on this AA revision consists of the following components:

| Device | Stepping | S-Spec Numbers |
|---|---|---|
| Intel Celeron 847 | Q0 | SR08N |
| Intel BD82QS77 | C1 | SLI8B |

# Specification Changes or Clarifications

Table 1 indicates the Specification Changes or Specification Clarifications that apply to the Intel® Desktop Board DCP847SKE.

**Table 1. Specification Changes or Clarifications**

| Date | Type of Change | Description of Changes or Clarifications |
|---|---|---|
| January 2013 | Spec Clarification | Deleted the note in Section 3.8 on page 60 regarding removing power before setting or clearing the hard disk drive password. |

# Errata

Current characterized errata, if any, are documented in a separate Specification Update. See http://developer.intel.com/products/desktop/motherboard/index.htm for the latest documentation.

# Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for Intel® Next Unit of Computing Board DCP847SKE.

## Intended Audience

The TPS is intended to provide detailed, technical information about Intel Next Unit of Computing Board DCP847SKE and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

## What This Document Contains

| Chapter | Description |
|---|---|
| 1 | A description of the hardware used on Intel Next Unit of Computing Board DCP847SKE |
| 2 | A map of the resources of the Intel Next Unit of Computing Board |
| 3 | The features supported by the BIOS Setup program |
| 4 | A description of the BIOS error messages, beep codes, and POST codes |
| 5 | Regulatory compliance and battery disposal information |

## Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

### Notes, Cautions, and Warnings

**NOTE**

*Notes call attention to important information.*

**CAUTION**

*Cautions are included to help you avoid damaging hardware or losing data.*

# Other Common Notation

| | |
|---|---|
| # | Used after a signal name to identify an active-low signal (such as USBP0#) |
| GB | Gigabyte (1,073,741,824 bytes) |
| GB/s | Gigabytes per second |
| Gb/s | Gigabits per second |
| KB | Kilobyte (1024 bytes) |
| Kb | Kilobit (1024 bits) |
| kb/s | 1000 bits per second |
| MB | Megabyte (1,048,576 bytes) |
| MB/s | Megabytes per second |
| Mb | Megabit (1,048,576 bits) |
| Mb/s | Megabits per second |
| TDP | Thermal Design Power |
| xxh | An address or data value ending with a lowercase h indicates a hexadecimal value. |
| x.x V | Volts. Voltages are DC unless otherwise specified. |
| * | This symbol is used to indicate third-party brands and names that are the property of their respective owners. |

# Contents

## 2 Technical Reference



## 3 Overview of BIOS Features



## 4 Error Messages and Blink Codes



## 5 Regulatory Compliance and Battery Disposal Information

## Figures



## Tables

# 1 Product Description

## 1.1 Overview

### 1.1.1 Feature Summary

Table 2 summarizes the major features of the board.

**Table 2. Feature Summary**

| | |
|---|---|
| **Form Factor** | 4.0 inches by 4.0 inches (101.60 millimeters by 101.60 millimeters) |
| **Processor** | • Soldered-down Intel® Celeron® processor 847 with up to 17 W TDP<br>— Integrated graphics<br>— Integrated memory controller |
| **Memory** | • Two 204-pin DDR3 SDRAM Small Outline Dual Inline Memory Module (SO-DIMM) sockets<br>• Support for DDR3 1333 MHz and DDR3 1066 MHz SO-DIMMs<br>• Support for 1 Gb, 2 Gb, and 4 Gb memory technology<br>• Support for up to 16 GB of system memory with two SO-DIMMs using 4 Gb memory technology<br>• Support for non-ECC memory<br>• Support for 1.35 V low voltage JEDEC memory |
| **Chipset** | Intel® QS77 Express Chipset consisting of the Intel® QS77 Express Platform Controller Hub (PCH) |
| **Graphics** | • Integrated graphics support for processors with Intel® Graphics Technology:<br>— Two High Definition Multimedia Interface* (HDMI*) back panel connectors |
| **Audio** | Intel® High Definition Audio via the HDMI v1.4a interfaces |
| **Peripheral Interfaces** | • USB 2.0 ports:<br>— Three front panel ports (via one dual-port internal header and one front panel connector)<br>— Two ports are implemented with vertical back panel connectors<br>— One port is reserved for the PCI Express* Half-Mini Card<br>— One port is reserved for the PCI Express Full-Mini Card<br>• SATA port:<br>— One internal mSATA port (PCI Express Full-Mini Card) for SSD support |
| **Expansion Capabilities** | • One PCI Express Half-Mini Card connector<br>• One PCI Express Full-Mini Card connector |
| **BIOS** | • Intel® BIOS resident in the Serial Peripheral Interface (SPI) Flash device<br>• Support for Advanced Configuration and Power Interface (ACPI), Plug and Play, and System Management BIOS (SMBIOS) |

continued

**Table 2. Feature Summary** (continued)

| | |
|---|---|
| **LAN Support** | Gigabit (10/100/1000 Mb/s) LAN subsystem using the Intel® 82579V Gigabit Ethernet Controller |
| **Hardware Monitor Subsystem** | Hardware monitoring subsystem, based on a Nuvoton NPCE791C embedded controller, including:<br>• Voltage sense to detect out of range power supply voltages<br>• Thermal sense to detect out of range thermal values<br>• One processor fan header<br>• Fan sense input used to monitor fan activity<br>• Simple fan speed control |

## 1.1.2 Board Layout (Top)

Figure 1 shows the location of the major components on the top-side of Intel Next Unit of Computing Board DCP847SKE.

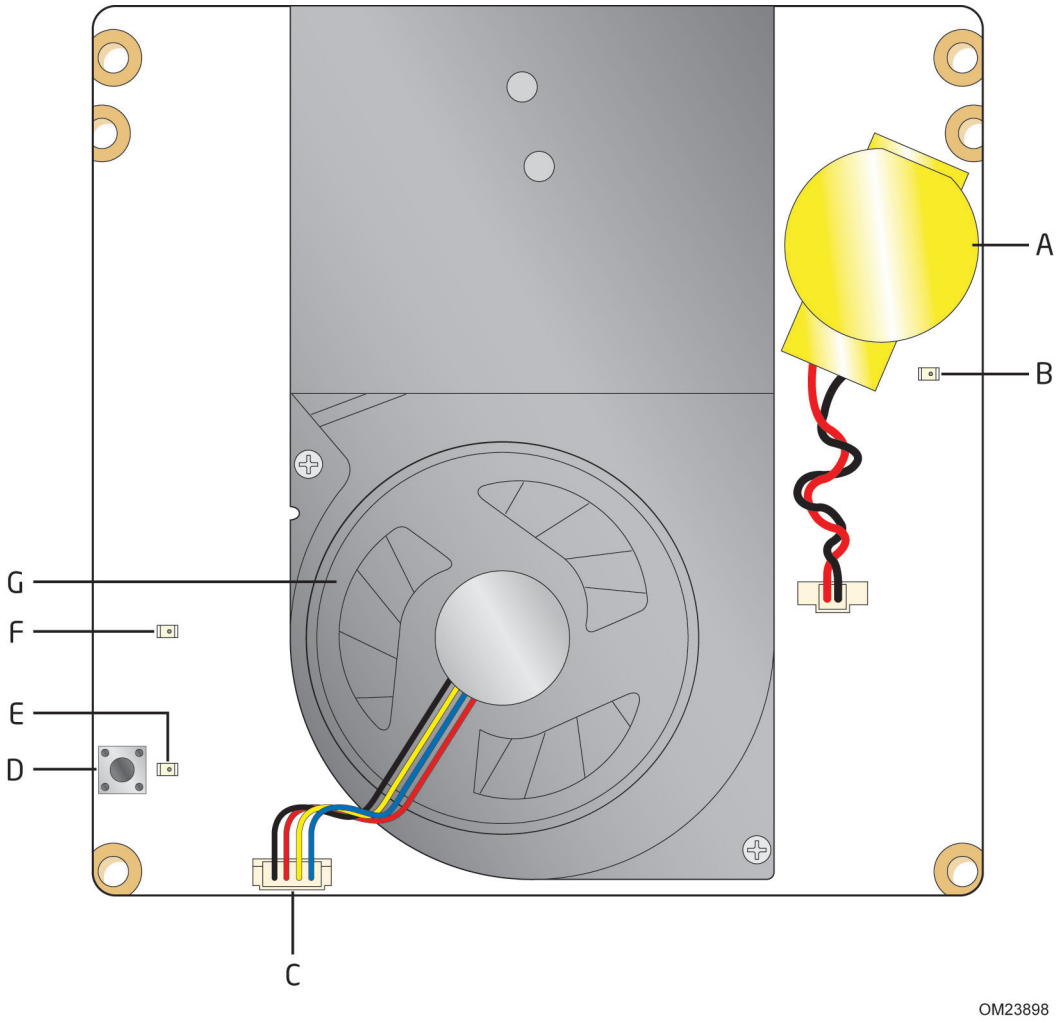



**Figure 1. Major Board Components (Top)**

Table 3 lists the components identified in Figure 1.

**Table 3. Components Shown in Figure 1**

| Item from Figure 1 | Description |
|---|---|
| A | Battery |
| B | Standby power LED |
| C | Processor fan header |
| D | Onboard power button |
| E | Power LED |
| F | Hard Disk Drive LED |
| G | Thermal solution |

### 1.1.3 Board Layout (Bottom)

Figure 2 shows the location of the major components on the bottom-side of Intel Next Unit of Computing Board DCP847SKE.

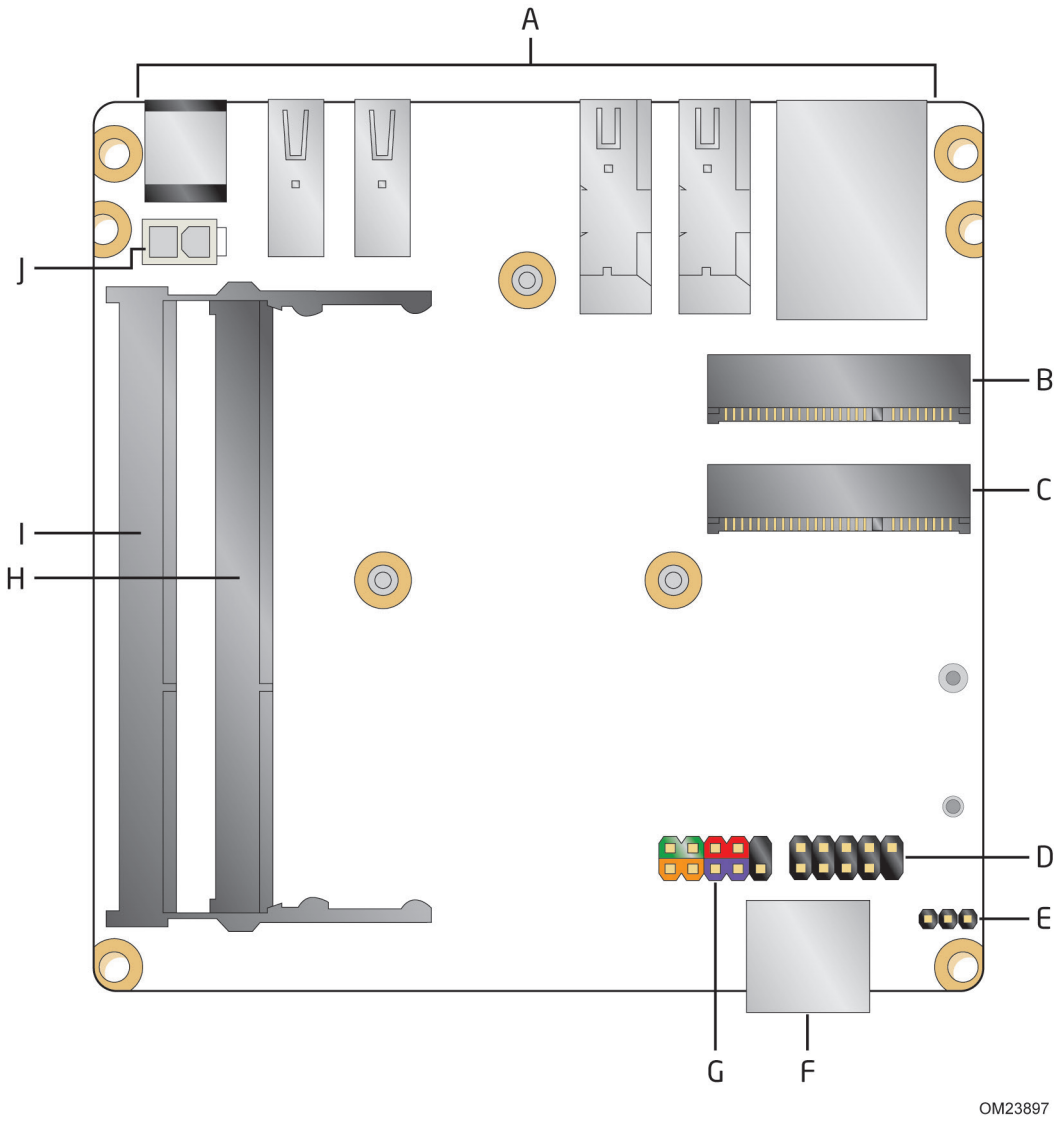



**Figure 2. Major Board Components (Bottom)**

**Table 4. Components Shown in Figure 2**

| Item from Figure 2 | Description |
|---|---|
| A | Back panel connectors |
| B | PCI Express Full-Mini Card connector |
| C | PCI Express Half-Mini Card connector |
| D | Front panel dual-port USB 2.0 header |
| E | BIOS setup configuration jumper |
| F | Front panel USB 2.0 connector |
| G | Front panel header |
| H | DDR3 SO-DIMM 2 socket |
| I | DDR3 SO-DIMM 1 socket |
| J | Internal DC power connector |

## 1.1.4 Block Diagram

Figure 3 is a block diagram of the major functional areas of the board.

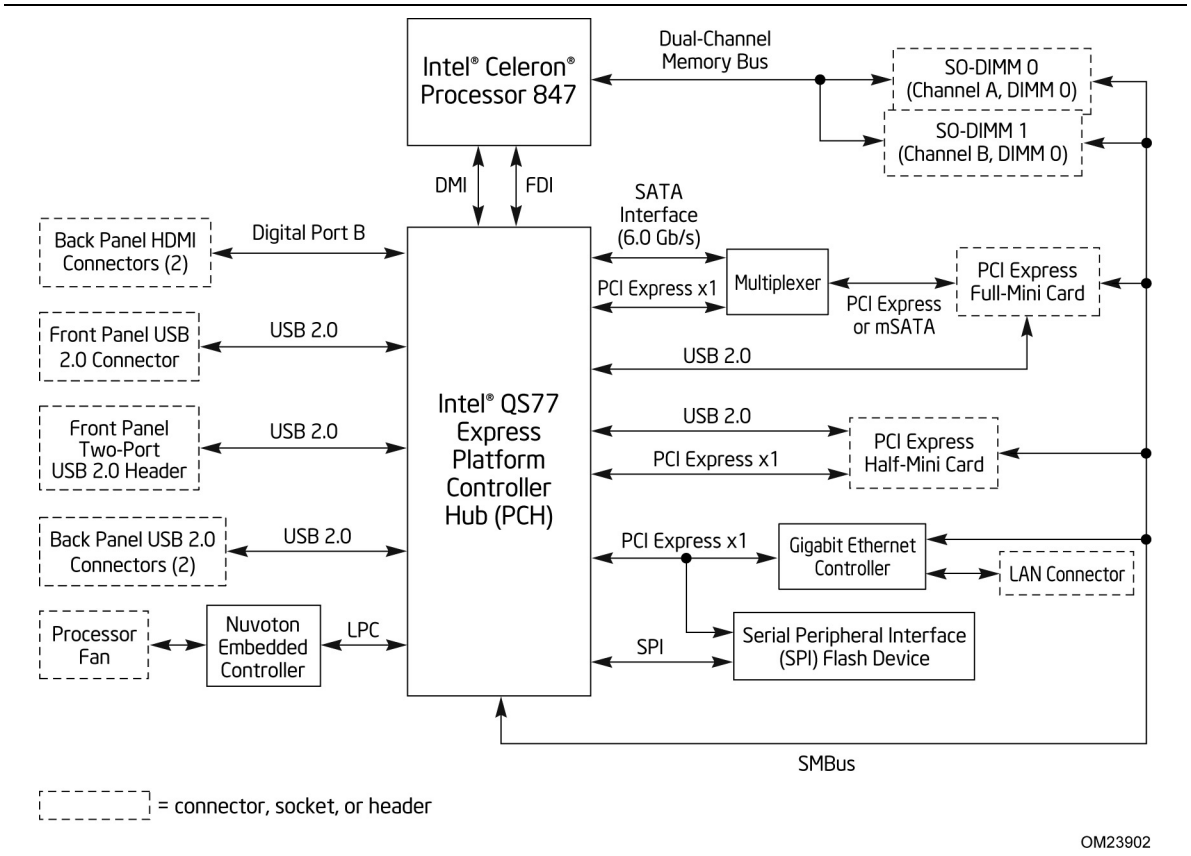



**Figure 3. Block Diagram**

## 1.2 Online Support

| To find information about… | Visit this World Wide Web site: |
|---|---|
| Intel Next Unit of Computing Board DCP847SKE | http://www.intel.com/products/motherboard/index.htm |
| Next Unit of Computing Board Support | http://www.intel.com/p/en_US/support?iid=hdr+support |
| Available configurations for Intel Next Unit of Computing Board DCP847SKE | http://ark.intel.com |
| Chipset information | http://www.intel.com/products/desktop/chipsets/index.htm |
| BIOS and driver updates | http://downloadcenter.intel.com |
| Tested memory | http://www.intel.com/support/motherboards/desktop/sb/CS-025414.htm |
| Integration information | http://www.intel.com/support/go/buildit |

## 1.3 Processor

The board has a soldered-down Intel Celeron processor 847 with Integrated Graphics Technology and integrated memory controller.

**NOTE**

*This board has specific requirements for providing power to the processor. Refer to Section 2.5.1 on page 49 for information on power supply requirements for this board.*

# 1.4 System Memory

The board has two 204-pin SO-DIMM sockets and supports the following memory features:

- 1.5 V DDR3 SDRAM SO-DIMMs with gold plated contacts
- Support for 1.35 V Low Voltage DDR3 (new JEDEC specification)
- Two independent memory channels with interleaved mode support
- Unbuffered, single-sided or double-sided SO-DIMMs
- 16 GB maximum total system memory (with 4 Gb memory technology). Refer to Section 2.1.1 on page 35 for information on the total amount of addressable memory.
- Minimum recommended total system memory: 1024 MB
- Non-ECC SO-DIMMs
- Serial Presence Detect
- XMP profile support for voltage detection
- DDR3 1333 MHz and DDR3 1066 MHz SDRAM SO-DIMMs

**NOTE**

*To be fully compliant with all applicable DDR SDRAM memory specifications, the board should be populated with SO-DIMMs that support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance. If non-SPD memory is installed, the BIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted or the SO-DIMMs may not function under the determined frequency.*

Table 5 lists the supported SO-DIMM configurations.

**Table 5. Supported Memory Configurations**

| Raw Card Version | SO-DIMM Capacity | DRAM Device Technology | DRAM Organization | # of DRAM Devices |
|---|---|---|---|---|
| A | 1 GB | 1 Gb | 64 M x 16 | 8 |
| | 2 GB | 2 Gb | 128 M x 16 | 8 |
| B | 1 GB | 1 Gb | 128 M x 8 | 8 |
| | 2 GB | 2 Gb | 256 M x 8 | 8 |
| C | 512 MB | 1 Gb | 64 M x 16 | 4 |
| | 1 GB | 2 Gb | 128 M x 16 | 4 |
| F | 2 GB | 1 Gb | 128 M x 8 | 16 |
| | 4 GB | 2 Gb | 256 M x 8 | 16 |
| | 8 GB | 4 Gb | 512 M x 8 | 16 |

Note: System memory configurations are based on availability and are subject to change.

| For information about… | Refer to: |
|---|---|
| Tested Memory | http://support.intel.com/support/motherboards/desktop/sb/CS-025414.htm |

### 1.4.1 Memory Configurations

The processor supports the following types of memory organization:

- **Dual channel (Interleaved) mode**. This mode offers the highest throughput for real world applications. Dual channel mode is enabled when the installed memory capacities of both SO-DIMM channels are equal. Technology and device width can vary from one channel to the other but the installed memory capacity for each channel must be equal. If different speed SO-DIMMs are used between channels, the slowest memory timing will be used.
- **Single channel (Asymmetric) mode**. This mode is equivalent to single channel bandwidth operation for real world applications. This mode is used when only a single SO-DIMM is installed or the memory capacities are unequal. Technology and device width can vary from one channel to the other. If different speed SO-DIMMs are used between channels, the slowest memory timing will be used.

| For information about… | Refer to: |
|---|---|
| Memory Configuration Examples | http://www.intel.com/support/motherboards/desktop/sb/cs-011965.htm |

Figure 4 illustrates the memory channel and SO-DIMM configuration.

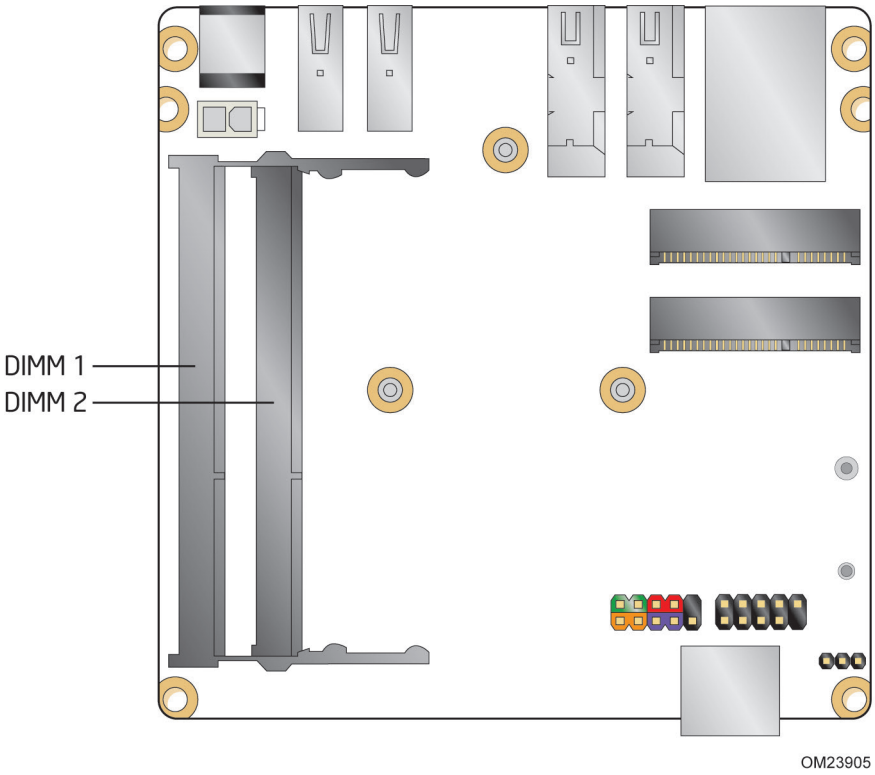



**Figure 4. Memory Channel and SO-DIMM Configuration**

# 1.5 Intel® QS77 Express Chipset

Intel QS77 Express Chipset with Direct Media Interface (DMI) interconnect provides interfaces to the processor and the USB, SATA, LPC, LAN, and PCI Express interfaces. The Intel QS77 Express Chipset is a centralized controller for the board's I/O paths.

| For information about | Refer to |
|---|---|
| The Intel QS77 chipset | http://www.intel.com/products/desktop/chipsets/index.htm |
| Resources used by the chipset | Chapter 2 |

## 1.5.1 Direct Media Interface (DMI)

Direct Media Interface (DMI) is the chip-to-chip connection between the processor and PCH. This high-speed interface integrates advanced priority-based servicing allowing for concurrent traffic and true isochronous transfer capabilities.

## 1.5.2 Display Interfaces

Display is divided between the processor and the PCH. The processor houses the memory interface, display planes, and pipes while the PCH has transcoder and display interface or ports. The PCH receives the display data over Intel® Flexible Display Interface (Intel® FDI) and transcodes the data as per the display technology protocol and sends the data through the display interface.

### 1.5.2.1 Intel® Flexible Display Interconnect (Intel® FDI)

Intel FDI connects the display engine in the processor with the display interfaces on the PCH. The display data from the frame buffer is processed in the display engine of the processor and sent to the PCH over the Intel FDI where it is transcoded as per the display protocol and driven to the display monitor.

### 1.5.2.2 High-bandwidth Digital Content Protection (HDCP)

HDCP is the technology for protecting high definition content against unauthorized copy or unreceptive between a source (computer, digital set top boxes, etc.) and the sink (panels, monitor, and TVs). The PCH supports HDCP 1.4 for content protection over wired displays (HDMI).

# 1.6 Graphics Subsystem

The board supports graphics through Intel Graphics Technology.

## 1.6.1 Integrated Graphics

The board supports integrated graphics through Intel FDI.

#### 1.6.1.1 Intel® High Definition (Intel® HD) Graphics

The Intel HD graphics controller features the following:

- 3D Features
  - DirectX* 10.1 and OpenGL* 3.0 compliant
  - DirectX 11.0 CS4.0 only
  - Shader Model 4.0
- Video
  - High-Definition content at up to 1080p resolution
  - Hardware accelerated MPEG-2, VC-1/WMV and H.264/AVC Hi-Definition video formats
  - Intel HD Technology with Advanced Hardware Video Transcoding
  - Blu-ray* S3D via HDMI 1.4a
  - Dynamic Video Memory Technology (DVMT) 5.0 support
  - Support of up to 1.7 GB Video Memory with 4 GB and above system memory configuration

#### 1.6.1.2 Video Memory Allocation

Intel® Dynamic Video Memory Technology (DVMT) is a method for dynamically allocating system memory for use as graphics memory to balance 2D/3D graphics and system performance. If your computer is configured to use DVMT, graphics memory is allocated based on system requirements and application demands (up to the configured maximum amount). When memory is no longer needed by an application, the dynamically allocated portion of memory is returned to the operating system for other uses.

#### 1.6.1.3 High Definition Multimedia Interface* (HDMI*)

The two HDMI ports support standard, enhanced, or high definition video, plus multi-channel digital audio on a single cable. Each port is compatible with all ATSC and DVB HDTV standards and supports eight full range channels at 24-bit/96 kHz audio of lossless audio formats such as Dolby* TrueHD or DTS* HD Master Audio. The maximum supported resolution is 1920 x 1200 (WUXGA). The HDMI port is compliant with the HDMI 1.4a specification.

##### 1.6.1.3.1 Integrated Audio Provided by the HDMI Interfaces

The following audio technologies are supported by the HDMI 1.4a interfaces directly from the PCH:

- AC-3 - Dolby* Digital
- Dolby Digital Plus
- DTS-HD*
- LPCM, 192 kHz/24-bit, 8 Channel

**NOTE**

*The PCH only supports one audio stream at a time over HDMI. Dual audio signals are not supported.*

### 1.6.2 USB

The board supports seven USB 2.0 ports. The port arrangement is as follows:

- Three front panel ports (via one dual-port internal header and one front panel connector)
- Two ports are implemented with vertical back panel connectors
- One port is reserved for the PCI Express Half-Mini Card
- One port is reserved for the PCI Express Full-Mini Card

All seven USB 2.0 ports are high-speed, full-speed, and low-speed capable.

**NOTE**

*Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device is attached to the cable. Use a shielded cable that meets the requirements for full-speed devices.*

| For information about | Refer to |
|---|---|
| The location of the USB connectors on the back panel | Figure 9, page 38 |
| The location of the front panel USB headers | Figure 2, page 15 |

## 1.7 SATA Interface

The board provides one internal mSATA port (PCI Express Full-Mini Card connector) for SSD support.

The PCH provides independent SATA ports with a theoretical maximum transfer rate of 6 Gb/s. A point-to-point interface is used for host to device connections.

The underlying SATA functionality is transparent to the operating system. The SATA controller can operate in both legacy and native modes. In legacy mode, standard IDE I/O and IRQ resources are assigned (IRQ 14 and 15). In Native mode, standard PCI Conventional bus resource steering is used. Native mode is the preferred mode for configurations using Windows operating systems.

### 1.7.1 AHCI Mode

The board supports AHCI storage mode via the Intel QS77 Express Chipset.

**NOTE**

*In order to use AHCI mode, AHCI must be enabled in the BIOS. Also, during Microsoft Windows XP installation, F6 must be pressed to install the AHCI drivers. See your Microsoft Windows XP documentation for more information about installing drivers during installation. Microsoft Windows 7 includes the necessary AHCI drivers without the need to install separate AHCI drivers during the operating system installation process, however, it is always good practice to update the AHCI drivers to the latest available by Intel.*

# 1.8 Real-Time Clock Subsystem

A coin-cell battery (CR2032) powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSB applied via the power supply 5 V STBY rail.

**NOTE**

*If the battery and AC power fail, date and time values will be reset and the user will be notified during the POST.*

When the voltage drops below a certain level, the BIOS Setup program settings stored in CMOS RAM (for example, the date and time) might not be accurate. Replace the battery with an equivalent one. Figure 1 on page 13 shows the location of the battery.

# 1.9 LAN Subsystem

The LAN subsystem consists of the following:

- Intel 82579V Gigabit Ethernet Controller (10/100/1000 Mb/s)
- Intel QS77 Express Chipset
- RJ-45 LAN connector with integrated status LEDs

Additional features of the LAN subsystem include:

- CSMA/CD protocol engine
- Jumbo frame support
- LAN connect interface between the PCH and the LAN controller
- Power management capabilities
  - ACPI technology support
  - LAN wake capabilities
- LAN subsystem software

| For information about | Refer to |
|---|---|
| LAN software and drivers | http://downloadcenter.intel.com |

### 1.9.1 Intel® 82579V Gigabit Ethernet Controller

The Intel 82579V Gigabit Ethernet Controller supports the following features:

- 10/100/1000 BASE-T IEEE 802.3 compliant
- Energy Efficient Ethernet (EEE) IEEE802.3az support (Low Power Idle (LPI) mode)
- Dual interconnect between the Integrated LAN Controller and the Physical Layer (PHY):
  - PCI Express-based interface for active state operation (S0) state
  - SMBUS for host and management traffic (Sx low power state)
- Compliant to IEEE 802.3x flow control support
- 802.1p and 802.1q
- TCP, IP, and UDP checksum offload (for IPv4 and IPv6)
- Full device driver compatibility

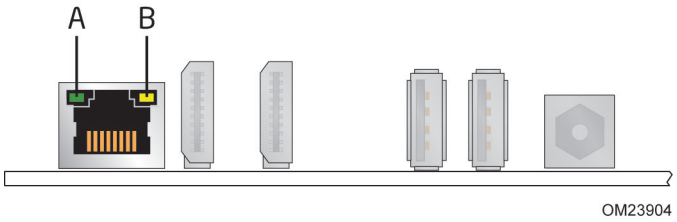
### 1.9.2 LAN Subsystem Software

LAN software and drivers are available from Intel's World Wide Web site.

| For information about | Refer to |
|---|---|
| Obtaining LAN software and drivers | http://downloadcenter.intel.com |

### 1.9.3 RJ-45 LAN Connector with Integrated LEDs

Two LEDs are built into the RJ-45 LAN connector (shown in Figure 5).




| Item | Description |
|---|---|
| A | Link LED (Green) |
| B | Data Rate LED (Green/Yellow) |

**Figure 5. LAN Connector LED Locations**

Table 6 describes the LED states when the board is powered up and the LAN subsystem is operating.

**Table 6. LAN Connector LED States**

| LED | LED Color | LED State | Condition |
|---|---|---|---|
| Link | Green | Off | LAN link is not established. |
| | | On | LAN link is established. |
| | | Blinking | LAN activity is occurring. |
| Data Rate | Green/Yellow | Off | 10 Mb/s data rate is selected. |
| | | Green | 100 Mb/s data rate is selected. |
| | | Yellow | 1000 Mb/s data rate is selected. |

# 1.10 Hardware Management Subsystem

The hardware management features enable the board to be compatible with the Wired for Management (WfM) specification. The board has several hardware management features, including thermal and voltage monitoring.

| For information about | Refer to |
|---|---|
| Wired for Management (WfM) Specification | www.intel.com/design/archives/wfm/ |

## 1.10.1 Hardware Monitoring

The hardware monitoring and fan control subsystem is based on a Nuvoton NPCE791C embedded controller, which supports the following:

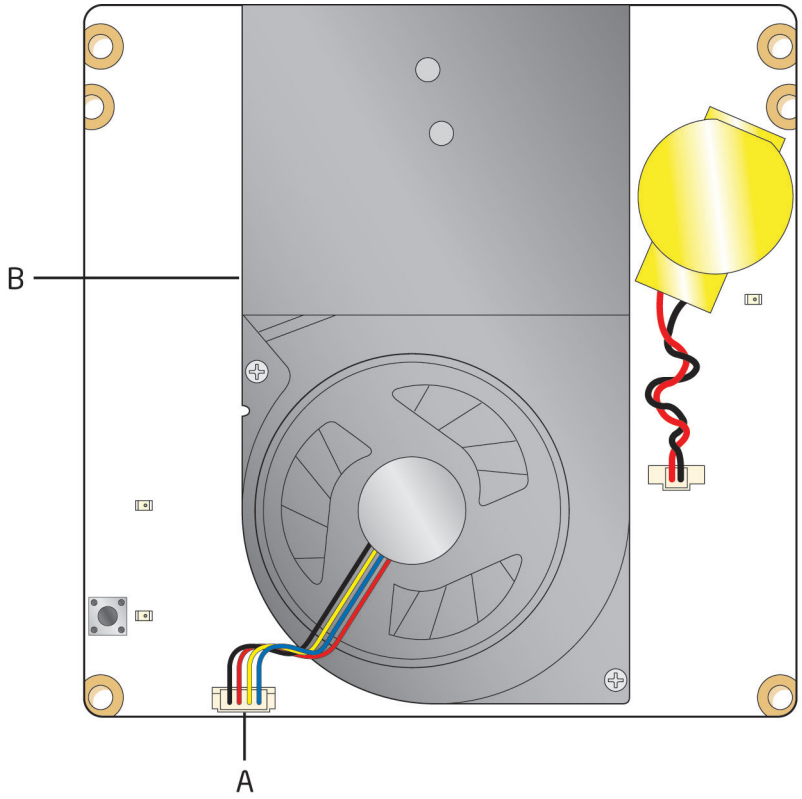
- Processor and system ambient temperature monitoring
- Chassis fan speed monitoring
- Voltage monitoring of +12 V, +5 V, +3.3 V, Memory Vcc (V_SM), +Vccp, PCH Vcc
- SMBus interface

## 1.10.2 Fan Monitoring

Fan monitoring can be implemented using third-party software.

## 1.10.3 Thermal Solution

Figure 6 shows the location of the thermal solution and processor fan header.




| Item | Description |
|---|---|
| A | Processor fan header |
| B | Thermal solution |

**Figure 6. Thermal Solution and Fan Header**

# 1.11 Power Management

Power management is implemented at several levels, including:

- Software support through Advanced Configuration and Power Interface (ACPI)
- Hardware support:
  - Power Input
  - Instantly Available PC technology
  - LAN wake capabilities
  - Wake from USB
  - WAKE# signal wake-up support
  - Wake from S5
  - +5 V Standby Power Indicator LED

## 1.11.1 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with this board requires an operating system that provides full ACPI support. ACPI features include:

- Plug and Play (including bus and device enumeration)
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 15-watt system operation in the power-on/standby sleeping state
- A Soft-off feature that enables the operating system to power-off the computer
- Support for multiple wake-up events (see Table 9 on page 32)
- Support for a front panel power and sleep mode switch

Table 7 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

**Table 7. Effects of Pressing the Power Switch**

| If the system is in this state… | …and the power switch is pressed for | …the system enters this state |
|---|---|---|
| Off<br>(ACPI G2/G5 – Soft off) | Less than four seconds | Power-on<br>(ACPI G0 – working state) |
| On<br>(ACPI G0 – working state) | Less than four seconds | Soft-off/Standby<br>(ACPI G1 – sleeping state) Note |
| On<br>(ACPI G0 – working state) | More than six seconds | Fail safe power-off<br>(ACPI G2/G5 – Soft off) |
| Sleep<br>(ACPI G1 – sleeping state) | Less than four seconds | Wake-up<br>(ACPI G0 – working state) |
| Sleep<br>(ACPI G1 – sleeping state) | More than six seconds | Power-off<br>(ACPI G2/G5 – Soft off) |

Note: Depending on power management settings in the operating system.

### 1.11.1.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 8 lists the power states supported by the board along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

**Table 8. Power States and Targeted System Power**

| Global States | Sleeping States | Processor States | Device States | Targeted System Power (Note 1) |
|---|---|---|---|---|
| G0 – working state | S0 – working | C0 – working | D0 – working state. | Full power > 30 W |
| G1 – sleeping state | S3 – Suspend to RAM. Context saved to RAM. | No power | D3 – no power except for wake-up logic. | Power < 5 W (Note 2) |
| G1 – sleeping state | S4 – Suspend to disk. Context saved to disk. | No power | D3 – no power except for wake-up logic. | Power < 5 W (Note 2) |
| G2/S5 | S5 – Soft off. Context not saved. Cold boot is required. | No power | D3 – no power except for wake-up logic. | Power < 5 W (Note 2) |
| G3 – mechanical off<br>AC power is disconnected from the computer. | No power to the system. | No power | D3 – no power for wake-up logic, except when provided by battery or external source. | No power to the system. Service can be performed safely. |

Notes:

1. Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.
2. Dependent on the standby power consumption of wake-up devices used in the system.

#### 1.11.1.2 Wake-up Devices and Events

Table 9 lists the devices or specific events that can wake the computer from specific states.

**Table 9. Wake-up Devices and Events**

| Devices/events that wake up the system… | …from this sleep state | …from this global state |
|---|---|---|
| Power switch | S3, S4, S5 (Note 1) | G1, G2, G3 |
| RTC alarm | S3, S4, S5 (Note 1) | G1, G2 (Note 3) |
| LAN | S3, S4, S5 (Note 1) | G1, G2 (Note 3) |
| USB | S3 | G1 |
| WAKE# | S3, S4, S5 (Note 1) | G1, G2 (Note 3) |

Notes:

1. S4 implies operating system support only.
2. Wake from S4 and S5 is recommended by Microsoft.
3. Wake from device/event not supported immediately upon return from AC loss.

**NOTE**

*The use of these wake-up events from an ACPI state requires an operating system that provides full ACPI support. In addition, software, drivers, and peripherals must fully support ACPI wake events.*

### 1.11.2 Hardware Support

The board provides several power management hardware features, including:

- Wake from Power Button signal
- Instantly Available PC technology
- LAN wake capabilities
- Wake from USB
- WAKE# signal wake-up support
- Wake from S5
- +5 V Standby Power Indicator LED

**NOTE**

*The use of Wake from USB from an ACPI state requires an operating system that provides full ACPI support.*

#### 1.11.2.1 Power Input

When resuming from an AC power failure, the computer returns to the power state it was in before power was interrupted (on or off). The computer's response can be set using the Last Power State feature in the BIOS Setup program's Boot menu.

| For information about | Refer to |
|---|---|
| The location of the internal power connector | Figure 2, page 15 |
| The signal names of the internal power connector | Table 14, page 43 |

#### 1.11.2.2 Instantly Available PC Technology

Instantly Available PC technology enables the board to enter the ACPI S3 (Suspend-to-RAM) sleep-state. While in the S3 sleep-state, the computer will appear to be off (the power supply is off, and the front panel LED is amber if dual colored, or off if single colored.) When signaled by a wake-up device or event, the system quickly returns to its last known wake state. Table 9 on page 32 lists the devices and events that can wake the computer from the S3 state.

The use of Instantly Available PC technology requires operating system support and drivers for any installed PCI Express add-in card.

#### 1.11.2.3 LAN Wake Capabilities

LAN wake capabilities enable remote wake-up of the computer through a network. The LAN subsystem monitors network traffic at the Media Independent Interface. Upon detecting a Magic Packet* frame, the LAN subsystem asserts a wake-up signal that powers up the computer.

#### 1.11.2.4 Wake from USB

USB bus activity wakes the computer from an ACPI S3 state.

**NOTE**

*Wake from USB requires the use of a USB peripheral that supports Wake from USB.*

#### 1.11.2.5 WAKE# Signal Wake-up Support

When the WAKE# signal on the PCI Express bus is asserted, the computer wakes from an ACPI S3, S4, or S5 state.

#### 1.11.2.6 Wake from S5

When the RTC Date and Time is set in the BIOS, the computer will automatically wake from an ACPI S5 state.

### 1.11.2.7 +5 V Standby Power Indicator LED

The standby power indicator LED shows that power is still present even when the computer appears to be off. Figure 7 shows the location of the standby power LED.

**CAUTION**

*If AC power has been switched off and the standby power indicator is still lit, disconnect the power cord before installing or removing any devices connected to the board. Failure to do so could damage the board and any attached devices.*

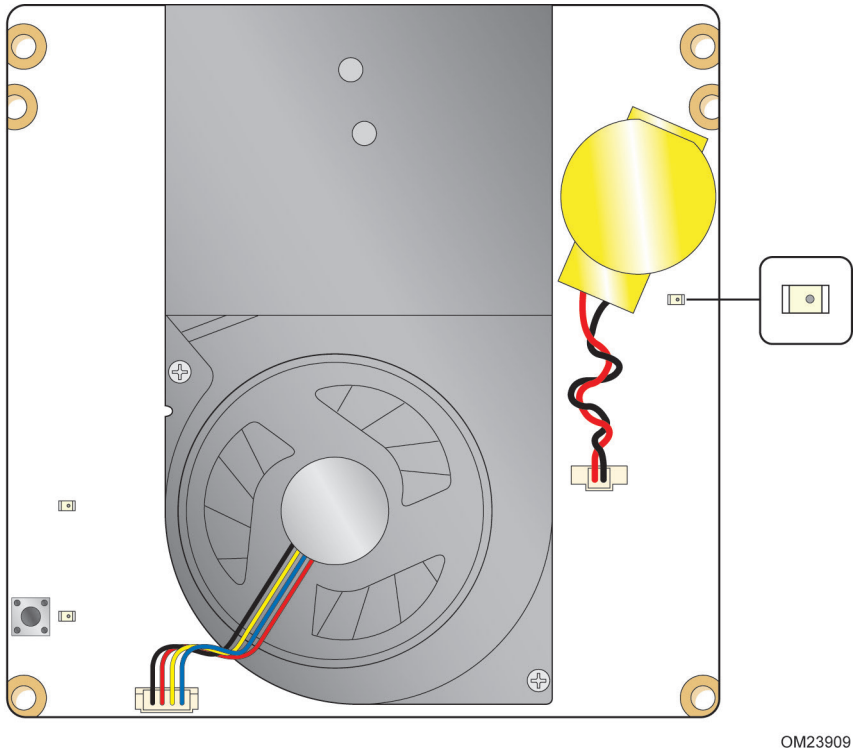



**Figure 7. Location of the Standby Power LED**

# 2 Technical Reference

## 2.1 Memory Resources

### 2.1.1 Addressable Memory

The board utilizes 16 GB of addressable system memory. Typically the address space that is allocated for PCI Conventional bus add-in cards, PCI Express configuration space, BIOS (SPI Flash device), and chipset overhead resides above the top of DRAM (total system memory). On a system that has 16 GB of system memory installed, it is not possible to use all of the installed memory due to system address space being allocated for other system critical functions. These functions include the following:

- BIOS/SPI Flash device (16 Mbit)
- Local APIC (19 MB)
- Direct Media Interface (40 MB)
- PCI Express configuration space (256 MB)
- PCH base address registers PCI Express ports (up to 256 MB)
- Memory-mapped I/O that is dynamically allocated for PCI Express add-in cards (256 MB)

The board provides the capability to reclaim the physical memory overlapped by the memory mapped I/O logical address space. The board remaps physical memory from the top of usable DRAM boundary to the 4 GB boundary to an equivalent sized logical address range located just above the 4 GB boundary. Figure 8 shows a schematic of the system memory map. All installed system memory can be used when there is no overlap of system addresses.

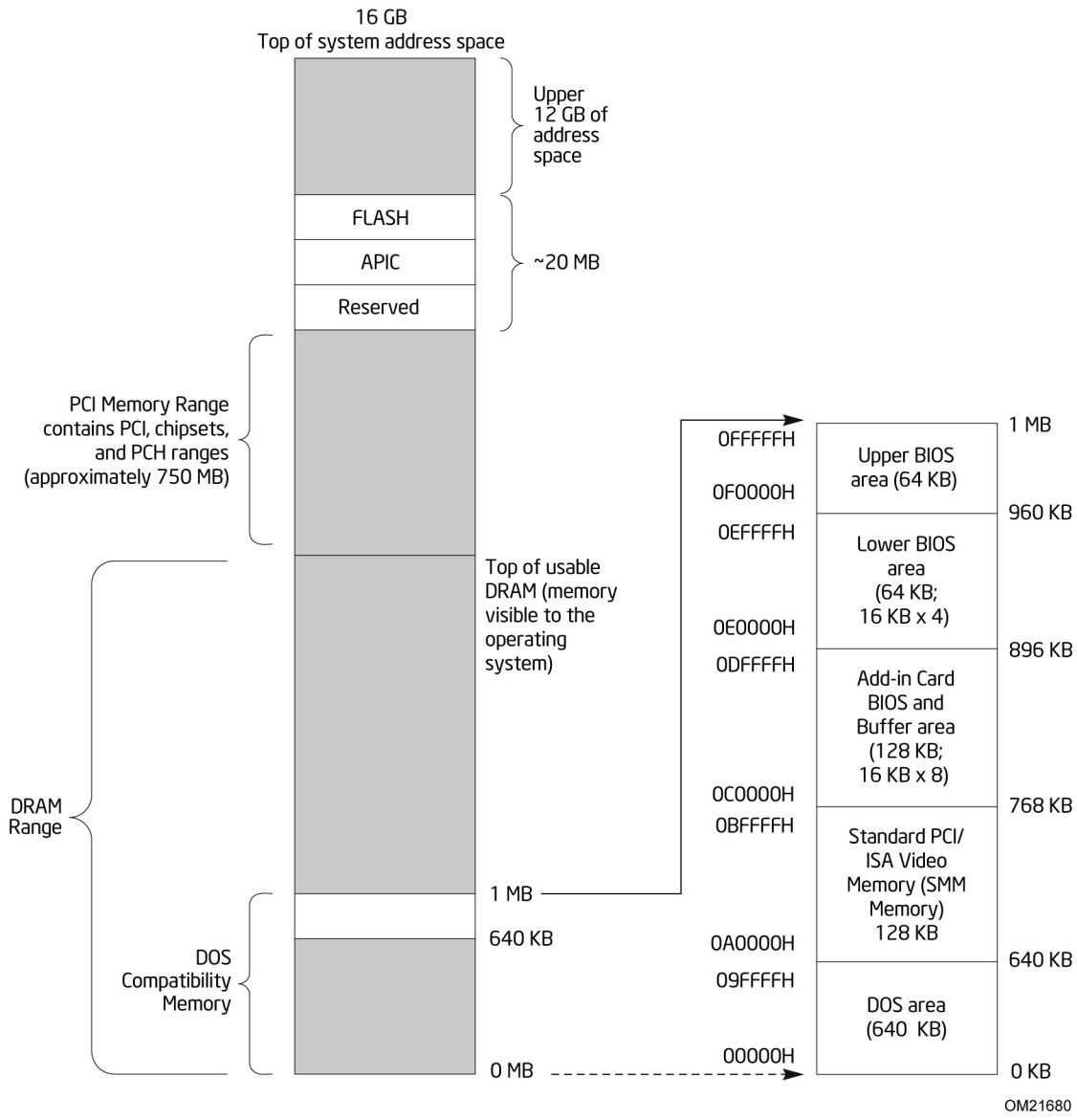



**Figure 8. Detailed System Memory Address Map**

### 2.1.2 Memory Map

Table 10 lists the system memory map.

**Table 10. System Memory Map**

| Address Range (decimal) | Address Range (hex) | Size | Description |
|---|---|---|---|
| 1024 K - 16777216 K | 100000 – 400000000 | 16382 MB | Extended memory |
| 960 K - 1024 K | F0000 - FFFFF | 64 KB | Runtime BIOS |
| 896 K - 960 K | E0000 - EFFFF | 64 KB | Reserved |
| 800 K - 896 K | C8000 - DFFFF | 96 KB | Potential available high DOS memory (open to the PCI Conventional bus). Dependent on video adapter used. |
| 640 K - 800 K | A0000 - C7FFF | 160 KB | Video memory and BIOS |
| 639 K - 640 K | 9FC00 - 9FFFF | 1 KB | Extended BIOS data (movable by memory manager software) |
| 512 K - 639 K | 80000 - 9FBFF | 127 KB | Extended conventional memory |
| 0 K - 512 K | 00000 - 7FFFF | 512 KB | Conventional memory |

## 2.2 Connectors and Headers

**CAUTION**

*Only the following connectors and headers have overcurrent protection: back panel and front panel USB.*

*The other internal connectors and headers are not overcurrent protected and should connect only to devices inside the computer's chassis, such as fans and internal peripherals. Do not use these connectors or headers to power devices external to the computer's chassis. A fault in the load presented by the external devices could cause damage to the computer, the power cable, and the external devices themselves.*

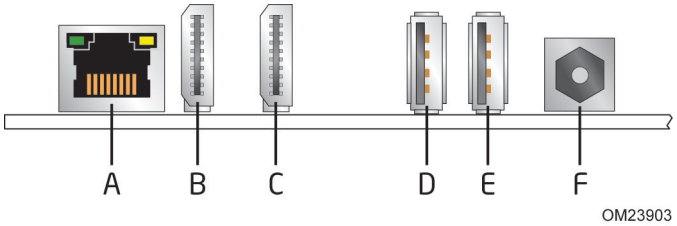
*Furthermore, improper connection of USB header single wire connectors may eventually overload the overcurrent protection and cause damage to the board.*

This section describes the board's connectors and headers. The connectors and headers can be divided into these groups:

- Back panel I/O connectors
- On-board I/O connectors and headers (see page 39)

## 2.2.1 Back Panel Connectors

Figure 9 shows the location of the back panel connectors for the board.




| Item | Description |
|---|---|
| A | LAN |
| B | HDMI connector 2 |
| C | HDMI connector 1 |
| D | USB 2.0 port |
| E | USB 2.0 port |
| F | 19 V DC input jack |

**Figure 9. Back Panel Connectors**

## 2.2.2 Connectors and Headers (Bottom)

Figure 10 shows the locations of the connectors and headers on the bottom-side of the board.

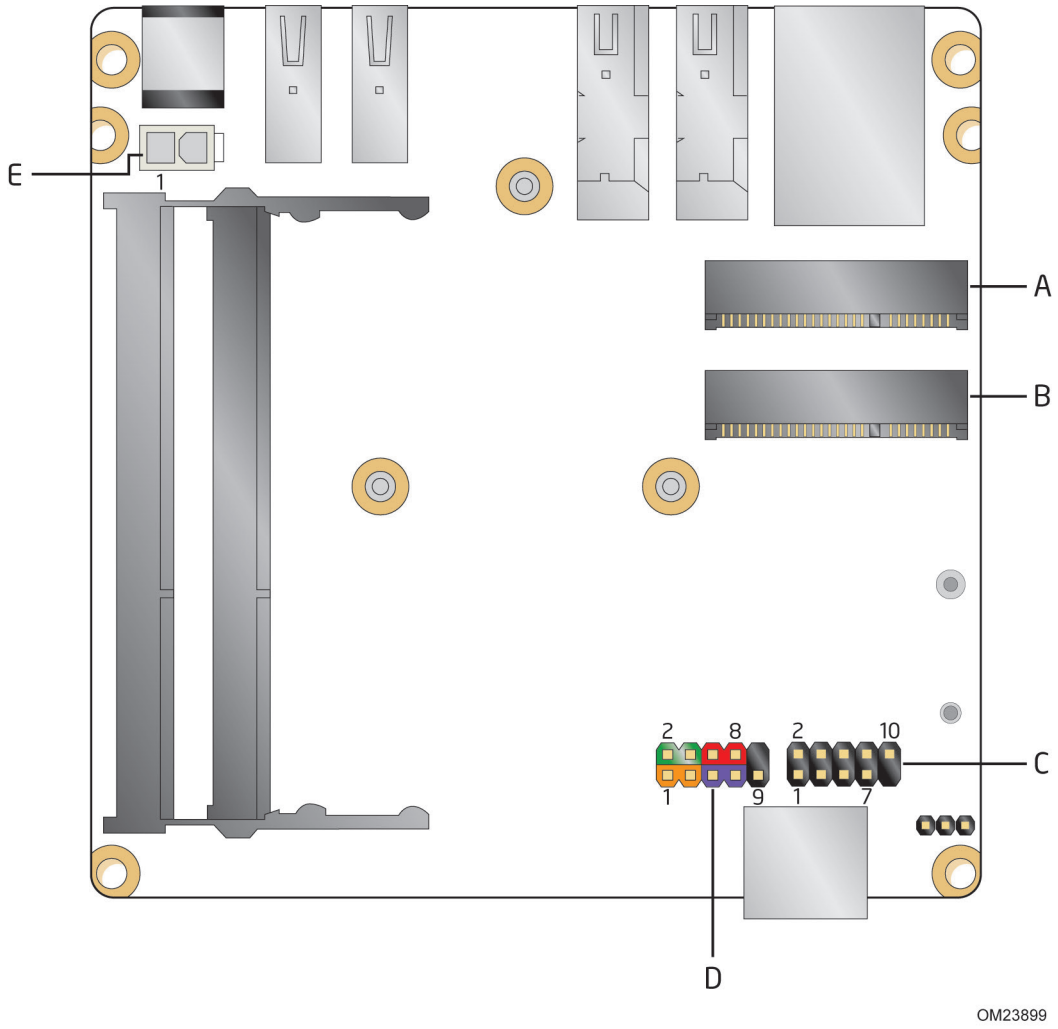



**Figure 10. Connectors and Headers (Bottom)**

Table 11 lists the connectors and headers identified in Figure 10.

**Table 11. Connectors and Headers Shown in Figure 10**

| Item from Figure 10 | Description |
|---|---|
| A | PCI Express Full-Mini Card connector |
| B | PCI Express Half-Mini Card connector |
| C | Front panel dual-port USB 2.0 header |
| D | Front panel header |
| E | Internal DC power connector |

### 2.2.2.1 Signal Tables for the Connectors and Headers

**Table 12. PCI Express Full-Mini Card Connector**

| Pin | Signal Name | Additional Signal Name |
|---|---|---|
| 1 | WAKE# | |
| 2 | 3.3 V | |
| 3 | Reserved | (Extra USB) +5 V_MINI |
| 4 | GND | |
| 5 | Reserved | (Extra USB) CARDIN |
| 6 | 1.5 V | |
| 7 | CLKREQ# | |
| 8 | Reserved | |
| 9 | GND | |
| 10 | Reserved | |
| 11 | REFCLK- | |
| 12 | Reserved | |
| 13 | REFCLK+ | |
| 14 | Reserved | |
| 15 | GND | |
| 16 | Reserved | |
| 17 | Reserved | (Extra USB) LP5- |
| 18 | GND | |
| 19 | Reserved | (Extra USB) LP5+ |
| 20 | Reserved | |
| 21 | GND | |
| 22 | PERST# | |
| 23 | PERn0 | |
| 24 | +3.3 V aux | |
| 25 | PERp0 | |
| 26 | GND | |
| 27 | GND | |
| 28 | +1.5 V | |
| 29 | GND | |
| 30 | SMB_CLK | |
| 31 | PETn0 | |
| 32 | SMB_DATA | |
| 33 | PETp0 | |
| 34 | GND | |
| 35 | GND | |
| 36 | USB_D- | |
| 37 | GND | |
| 38 | USB_D+ | |

continued

**Table 12. PCI Express Full-Mini Card Connector** (continued)

| Pin | Signal Name | Additional Signal Name |
|---|---|---|
| 39 | +3.3 Vaux | |
| 40 | GND | |
| 41 | +3.3 Vaux | |
| 42 | LED_WWAN# | |
| 43 | Reserved | |
| 44 | LED_WLAN# | |
| 45 | Reserved | (mSATA) Vendor |
| 46 | LED_WPAN# | |
| 47 | Reserved | (mSATA) Vendor |
| 48 | +1.5V | |
| 49 | Reserved | (mSATA) DA/DSS |
| 50 | GND | |
| 51 | Reserved | (mSATA) Presence Detection |
| 52 | +3.3V | |

**Table 13. Dual-Port Front Panel USB 2.0 Header**

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | +5 V DC | 2 | +5 V DC |
| 3 | D– | 4 | D– |
| 5 | D+ | 6 | D+ |
| 7 | Ground | 8 | Ground |
| 9 | KEY (no pin) | 10 | No Connect |

### 2.2.2.2 Add-in Card Connectors

The board has the following add-in card connectors:

- One PCI Express Half-Mini Card
- One PCI Express Full-Mini Card

### 2.2.2.3 Power Supply Connectors

The board has the following power supply connectors:

- **External Power Supply** – the board can be powered through a 19 V DC connector on the back panel. The back panel DC connector is compatible with a 5.5 mm/OD (outer diameter) and 2.5 mm/ID (inner diameter) plug, where the inner contact is +19 (±10%) V DC and the shell is GND. The maximum current rating is 10 A.
- **Internal Power Supply** – the board can alternatively be powered via the internal 19 V DC 1 x 2 power connector, where pin 1 is GND and pin 2 is +19 (±10%) VDC.

**Table 14. 19 V Internal Power Supply Connector**

| Pin | Signal Name |
|---|---|
| 1 | Ground |
| 2 | +19 V (±10%) |

| For information about | Refer to |
|---|---|
| Power supply considerations | Section 2.5.1, page 49 |

### 2.2.2.4 Front Panel Header

This section describes the functions of the front panel header. Table 15 lists the signal names of the front panel header. Figure 11 is a connection diagram for the front panel header.

**Table 15. Front Panel Header**

| Pin | Signal Name | Description | Pin | Signal Name | Description |
|---|---|---|---|---|---|
| 1 | HDD_POWER_LED | Pull-up resistor (750 Ω) to +5V | 2 | POWER_LED_MAIN | [Out] Front panel LED (main color) |
| 3 | HDD_LED# | [Out] Hard disk activity LED | 4 | POWER_LED_ALT | [Out] Front panel LED (alt color) |
| 5 | GROUND | Ground | 6 | POWER_SWITCH# | [In] Power switch |
| 7 | RESET_SWITCH# | [In] Reset switch | 8 | GROUND | Ground |
| 9 | +5V_DC | Power | 10 | Key | No pin |

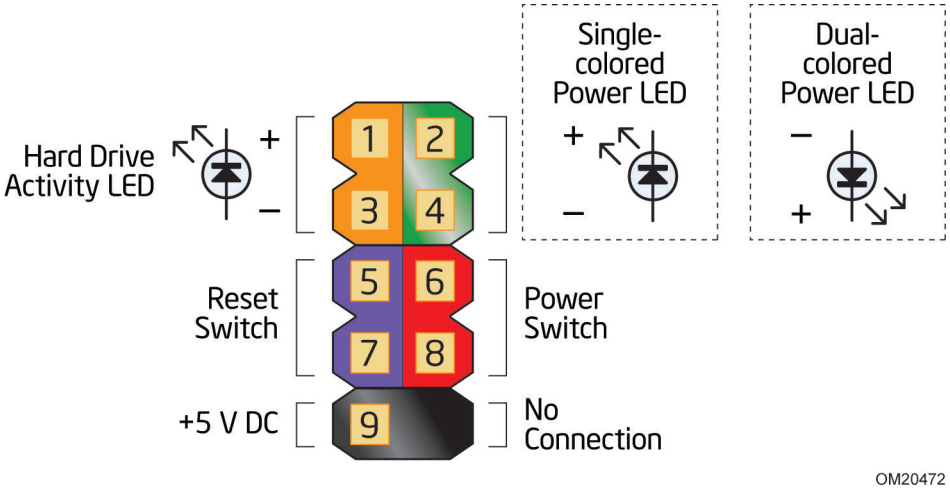



**Figure 11. Connection Diagram for Front Panel Header**

#### 2.2.2.4.1 Hard Drive Activity LED Header

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. Proper LED function requires a SATA hard drive or optical drive connected to an onboard SATA connector.

#### 2.2.2.4.2 Reset Switch Header

Pins 5 and 7 can be connected to a momentary single pole, single throw (SPST) type switch that is normally open. When the switch is closed, the board resets and runs the POST.

#### 2.2.2.4.3 Power/Sleep LED Header

Pins 2 and 4 can be connected to a one- or two-color LED. Table 16 shows the possible LED states.

**Table 16. States for a One-Color Power LED**

| LED State | Description |
|---|---|
| Off | Power off |
| Blinking | Standby |
| Steady | Normal operation |

**NOTE**

*The LED behavior shown in Table 16 is default – other patterns may be set via BIOS setup.*

#### 2.2.2.4.4 Power Switch Header

Pins 6 and 8 can be connected to a front panel momentary-contact power switch. The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the board.) At least two seconds must pass before the power supply will recognize another on/off signal.

### 2.2.2.5 Front Panel USB 2.0 Header

Figure 12 is a connection diagram for the front panel USB 2.0 header.

**NOTE**

- *The +5 V DC power on the USB header is fused.*
- *Use only a front panel USB connector that conforms to the USB 2.0 specification for high-speed USB devices.*

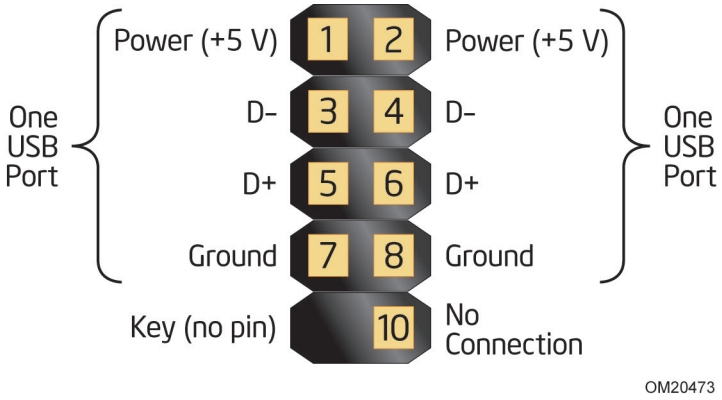



**Figure 12. Connection Diagram for Front Panel USB 2.0 Dual-Port Header**

# 2.3 BIOS Setup Configuration Jumper

**CAUTION**

*Do not move a jumper with the power on. Always turn off the power and unplug the power cord from the computer before changing a jumper setting. Otherwise, the board could be damaged.*

Figure 13 shows the location of the BIOS Setup Configuration jumper.

Table 17 describes the BIOS Setup configuration jumper settings for the three modes: normal, configure, and recovery. When the jumper is set to configure mode and the computer is powered-up, the BIOS compares the processor version and the microcode version in the BIOS and reports if the two match.

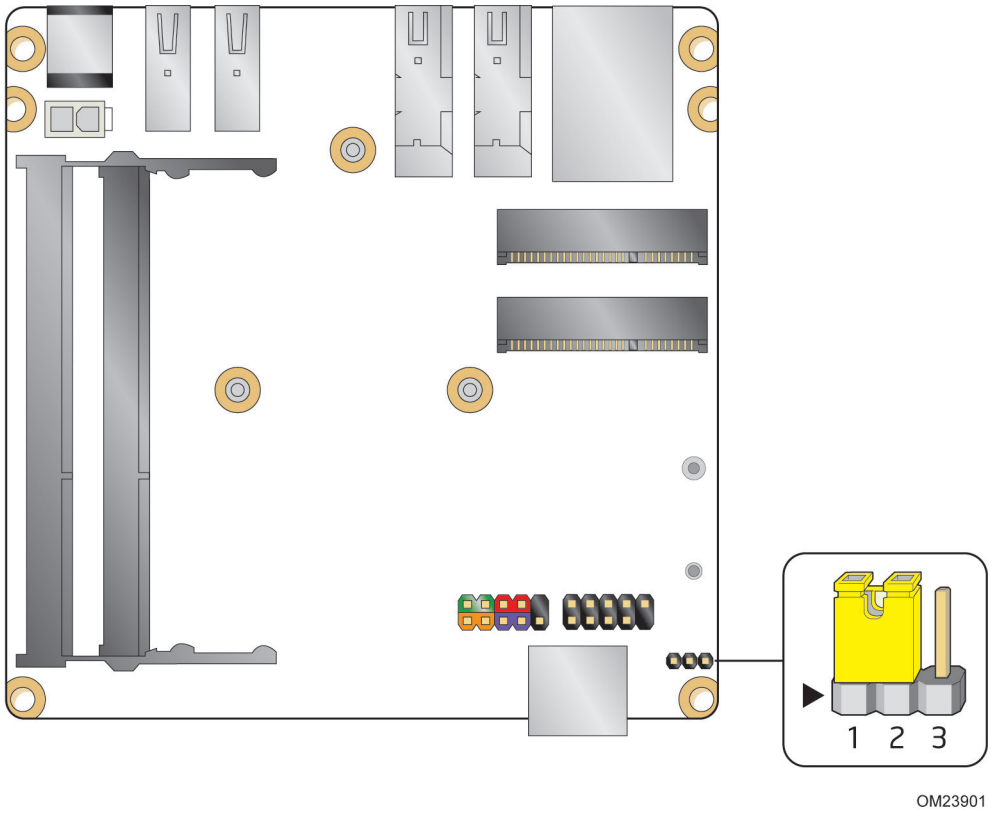



**Figure 13. Location of the BIOS Configuration Setup Jumper**

Table 17 lists the settings for the jumper.

**Table 17. BIOS Setup Configuration Jumper Settings**

| Function/Mode | Jumper Setting | Configuration |
|---|---|---|
| Normal | 1-2 | The BIOS uses current configuration information and passwords for booting. |
| Configure | 2-3 | After the POST runs, Setup runs automatically. The maintenance menu is displayed.<br><br>Note that this Configure mode is the only way to clear the BIOS/CMOS settings. Press F9 (restore defaults) while in Configure mode to restore the BIOS/CMOS settings to their default values. |
| Recovery | None | The BIOS attempts to recover the BIOS configuration. A recovery CD or flash drive is required. |

# 2.4 Mechanical Considerations

## 2.4.1 Form Factor

The board is designed to fit into a custom chassis. Figure 14 illustrates the mechanical form factor for the board. Dimensions are given in inches [millimeters]. The outer dimensions are 4.0 inches by 4.0 inches [101.60 millimeters by 101.60 millimeters].

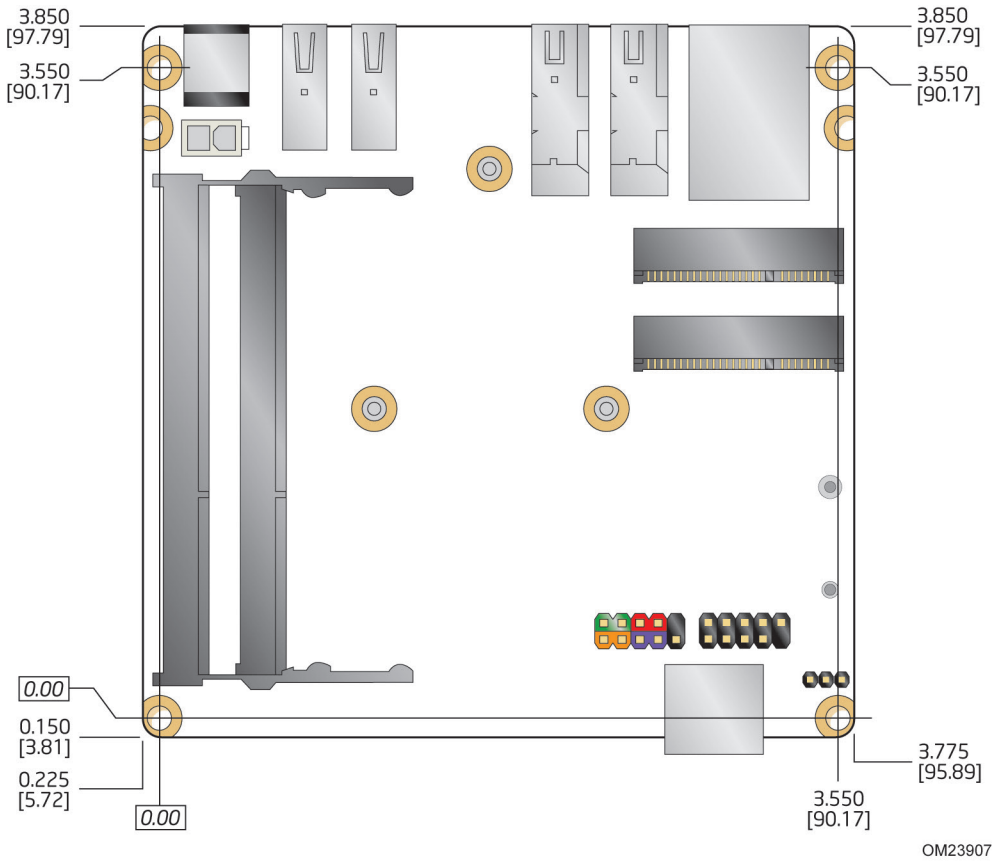



**Figure 14. Board Dimensions**

# 2.5 Electrical Considerations

## 2.5.1 Power Supply Considerations

**CAUTION**

*The external 19 V DC jack is the primary power input connector of Intel Next Unit of Computing Board DCP847SKE. However, the board also provides an internal 1 x 2 power connector that can be used in custom-developed systems that have an internal power supply.*

*There is no isolation circuitry between the external 19 V DC jack and the internal 1 x 2 power connector. It is the system integrator's responsibility to ensure no more than one power supply unit is or can be attached to the board at any time and to ensure the external 19 V DC jack is covered if the internal 1 x 2 power connector is to be used. A plastic lid for the external 19 V DC jack is provided in the accessories box shall it be useful to the system integrator for this purpose.*

*Simultaneous connection of both external and internal power supply units could result in potential damage to the board, power supplies, or other hardware.*

System power requirements will depend on actual system configurations chosen by the integrator, as well as end user expansion preferences. It is the system integrator's responsibility to ensure an appropriate power budget for the system configuration is properly assessed based on the system-level components chosen.

### 2.5.2 Fan Header Current Capability

Table 18 lists the current capability of the fan headers.

**Table 18. Fan Header Current Capability**

| Fan Header | Maximum Available Current |
|---|---|
| Processor fan | .1 A |

## 2.6 Thermal Considerations

**CAUTION**

*A chassis with a maximum internal ambient temperature of 58 °C at the processor fan inlet is a requirement. Whenever possible, use of a processor heat sink that provides omni-directional airflow to maintain required airflow across the processor voltage regulator area is recommended.*

**CAUTION**

*Failure to ensure appropriate airflow may result in reduced performance of both the processor and/or voltage regulator or, in some instances, damage to the board.*

*All responsibility for determining the adequacy of any thermal or system design remains solely with the system integrator. Intel makes no warranties or representations that merely following the instructions presented in this document will result in a system with adequate thermal performance.*

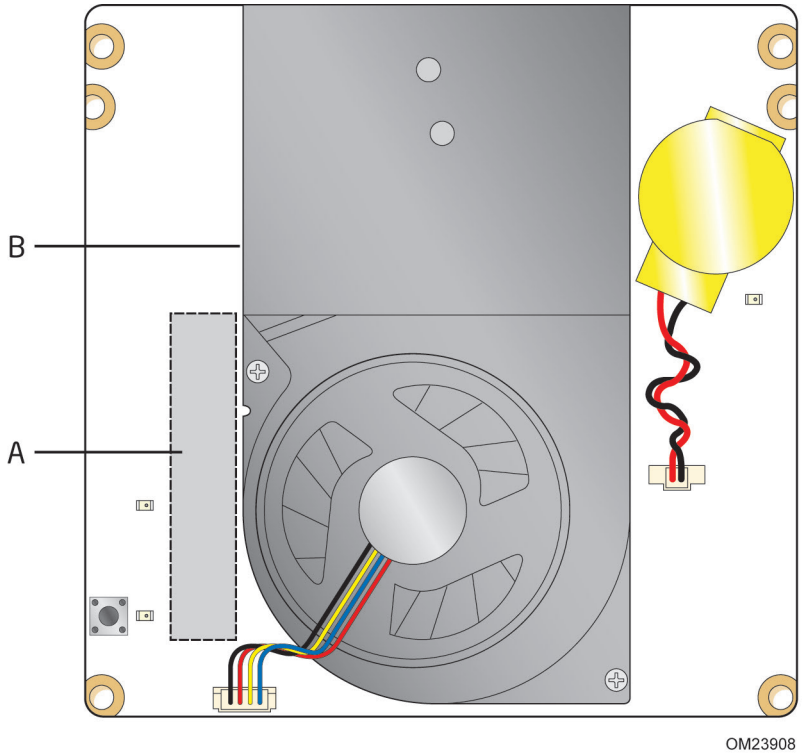
**CAUTION**

*Ensure that the ambient temperature does not exceed the board's maximum operating temperature. Failure to do so could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 2.8.*

**CAUTION**

*The processor voltage regulator area (shown in Figure 15) can reach a temperature of up to 97.5 °C in an open chassis. Ensure that proper airflow is maintained in the processor voltage regulator circuit. Failure to do so may result in shorter than expected product lifetime.*

Figure 15 shows the locations of the localized high temperature zones.




| Item | Description |
|---|---|
| A | Processor voltage regulator area |
| B | Thermal solution |

**Figure 15. Localized High Temperature Zones**

Table 19 provides maximum case temperatures for the components that are sensitive to thermal changes. The operating temperature, current load, or operating frequency could affect case temperatures. Maximum case temperatures are important when considering proper airflow to cool the board.

**Table 19. Thermal Considerations for Components**

| Component | Maximum Case Temperature |
|---|---|
| Processor | For processor case temperature, see processor datasheets and processor specification updates |
| Intel QS77 Express Chipset | 104 °C |

To ensure functionality and reliability, the component is specified for proper operation when Case Temperature is maintained at or below the maximum temperature listed in Table 20. This is a requirement for sustained power dissipation equal to Thermal Design Power (TDP is specified as the maximum sustainable power to be dissipated by the components). When the component is dissipating less than TDP, the case temperature should be below the Maximum Case Temperature. The surface temperature at the geometric center of the component corresponds to Case Temperature.

It is important to note that the temperature measurement in the system BIOS is a value reported by embedded thermal sensors in the components and does not directly correspond to the Maximum Case Temperature. The upper operating limit when monitoring this thermal sensor is Tcontrol.

**Table 20. Tcontrol Values for Components**

| Component | Tcontrol |
|---|---|
| Processor | For processor case temperature, see processor datasheets and processor specification updates |
| Intel QS77 Express Chipset | 104 °C |

| For information about | Refer to |
|---|---|
| Processor datasheets and specification updates | Section 1.2, page 18 |
| Intel® 7 Series Chipset Thermal Mechanical Specifications and Design Guidelines | http://www.intel.com/Products/Desktop/Chipsets/ec-QS77/QS77-technicaldocuments.htm |

# 2.7 Reliability

The Mean Time Between Failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Telcordia SR-332 Issue 2, Method I, Case 3, 55 ºC ambient. The MTBF prediction is used to estimate repair rates and spare parts requirements. The MTBF for the board is 90,936 hours.

# 2.8 Environmental

Table 21 lists the environmental specifications for the board.

**Table 21. Environmental Specifications**

| **Parameter** | **Specification** | | |
|---|---|---|---|
| **Temperature** | | | |
| Non-Operating | -40 °C to +60 °C | | |
| Operating | 0 °C to +50 °C | | |
| **Shock** | | | |
| Unpackaged | 50 g trapezoidal waveform | | |
| | Velocity change of 170 inches/s² | | |
| Packaged | Half sine 2 millisecond | | |
| | Product Weight (pounds) | Free Fall (inches) | Velocity Change (inches/s²) |
| | <20 | 36 | 167 |
| | 21-40 | 30 | 152 |
| | 41-80 | 24 | 136 |
| | 81-100 | 18 | 118 |
| **Vibration** | | | |
| Unpackaged | 5 Hz to 20 Hz: 0.01 g² Hz sloping up to 0.02 g² Hz | | |
| | 20 Hz to 500 Hz: 0.02 g² Hz (flat) | | |
| Packaged | 5 Hz to 40 Hz: 0.015 g² Hz (flat) | | |
| | 40 Hz to 500 Hz: 0.015 g² Hz sloping down to 0.00015 g² Hz | | |

# 3 Overview of BIOS Features

## 3.1 Introduction

The board uses a Intel Visual BIOS that is stored in the Serial Peripheral Interface Flash Memory (SPI Flash) and can be updated using a disk-based program. The SPI Flash contains the Visual BIOS Setup program, POST, the PCI auto-configuration utility, LAN EEPROM information, and Plug and Play support.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOSs are identified as GKPPT10H.86A.

When the BIOS Setup configuration jumper is set to configure mode and the computer is powered-up, the BIOS compares the CPU version and the microcode version in the BIOS and reports if the two match.

The Visual BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins.

**NOTE**

*The maintenance menu is displayed only when the board is in configure mode. Section 2.3 on page 46 shows how to put the board in configure mode.*

## 3.2 BIOS Flash Memory Organization

The Serial Peripheral Interface Flash Memory (SPI Flash) includes a 64 Mb (8192 KB) flash memory device.

## 3.3 System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information. Additional board information can be found in the BIOS under the Additional Information header under the Main BIOS page.

## 3.4 Legacy USB Support

Legacy USB support enables USB devices to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if Legacy USB support was set to Disabled in the BIOS Setup program.)

6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.
7. Additional USB legacy feature options can be access by using Intel® Integrator Toolkit.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

# 3.5 BIOS Updates

The BIOS can be updated using either of the following utilities, which are available on the Intel World Wide Web site:

- Intel® Express BIOS Update utility, which enables automated updating while in the Windows environment. Using this utility, the BIOS can be updated from a file on a hard disk, a USB drive (a flash drive or a USB hard drive), or a CD-ROM, or from the file location on the Web.
- Intel® Flash Memory Update Utility, which requires booting from DOS. Using this utility, the BIOS can be updated from a file on a hard disk, a USB drive (a flash drive or a USB hard drive), or a CD-ROM.
- Intel® F7 switch during POST allows a user to select where the BIOS .bio file is located and perform the update from that location/device. Similar to performing a BIOS Recovery without removing the BIOS configuration jumper.

Both utilities verify that the updated BIOS matches the target system to prevent accidentally installing an incompatible BIOS.

**NOTE**

*Review the instructions distributed with the upgrade utility before attempting a BIOS update.*

| For information about | Refer to |
|---|---|
| BIOS update utilities | http://support.intel.com/support/motherboards/desktop/sb/CS-022312.htm |

## 3.5.1 Language Support

The BIOS Setup program and help messages are supported in US English. Check the Intel web site for support.

### 3.5.2 Custom Splash Screen

During POST, an Intel® splash screen is displayed by default. This splash screen can be augmented with a custom splash screen. The Intel Integrator's Toolkit that is available from Intel can be used to create a custom splash screen.

**NOTE**

*If you add a custom splash screen, it will share space with the Intel branded logo.*

| For information about | Refer to |
|---|---|
| Intel Integrator Toolkit | http://developer.intel.com/design/motherbd/software/itk/ |
| Additional Intel® software tools | http://developer.intel.com/design/motherbd/software.htm |

## 3.6 BIOS Recovery

It is unlikely that anything will interrupt a BIOS update; however, if an interruption occurs, the BIOS could be damaged. Table 22 lists the drives and media types that can and cannot be used for BIOS recovery. The BIOS recovery media does not need to be made bootable.

**Table 22. Acceptable Drives/Media Types for BIOS Recovery**

| Media Type (Note) | Can be used for BIOS recovery? |
|---|---|
| Hard disk drive (connected to SATA or USB) | Yes |
| CD/DVD drive (connected to SATA or USB) | Yes |
| USB flash drive | Yes |
| USB diskette drive (with a 1.4 MB diskette) | No (BIOS update file is bigger than 1.4 MB size limit) |

**NOTE**

*Supported file systems for BIOS recovery:*

- *NTFS (sparse, compressed, or encrypted files are not supported)*
- *FAT32*
- *FAT16*
- *FAT12*
- *ISO 9660*

| For information about | Refer to |
|---|---|
| BIOS recovery | http://www.intel.com/support/motherboards/desktop/sb/cs-023360.htm |

# 3.7 Boot Options

In the BIOS Setup program, the user can choose to boot from a hard drive, optical drive, removable drive, or the network. The default setting is for the optical drive to be the first boot device, the hard drive second, removable drive third, and the network fourth.

## 3.7.1 Network Boot

The network can be selected as a boot device. This selection allows booting from the onboard LAN or a network add-in card with a remote boot ROM installed.

Pressing the <F12> key during POST automatically forces booting from the LAN. To use this key during POST, the User Access Level in the BIOS Setup program's Security menu must be set to Full.

## 3.7.2 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the following devices are not present:

- Video adapter
- Keyboard
- Mouse

## 3.7.3 Changing the Default Boot Device During POST

Pressing the <F10> key during POST causes a boot device menu to be displayed. This menu displays the list of available boot devices. Table 23 lists the boot device menu options.

**Table 23. Boot Device Menu Options**

| Boot Device Menu Function Keys | Description |
|---|---|
| <↑> or <↓> | Selects a default boot device |
| <Enter> | Exits the menu, and boots from the selected device |
| <Esc> | Exits the menu and boots according to the boot priority defined through BIOS setup |

# 3.8 Hard Disk Drive Password Security Feature

The Hard Disk Drive Password Security feature blocks read and write accesses to the hard disk drive until the correct password is given. Hard Disk Drive Passwords are set in BIOS SETUP and are prompted for during BIOS POST. For convenient support of S3 resume, the system BIOS will automatically unlock drives on resume from S3.

The User hard disk drive password, when installed, will be required upon each power-cycle until the Master Key or User hard disk drive password is submitted.

The Master Key hard disk drive password, when installed, will not lock the drive. The Master Key hard disk drive password exists as an unlock override in the event that the User hard disk drive password is forgotten. Only the installation of the User hard disk drive password will cause a hard disk to be locked upon a system power-cycle.

Table 24 shows the effects of setting the Hard Disk Drive Passwords.

**Table 24. Master Key and User Hard Drive Password Functions**

| Password Set | Password During Boot |
|---|---|
| Neither | None |
| Master only | None |
| User only | User only |
| Master and User Set | Master or User |

During every POST, if a User hard disk drive password is set, POST execution will pause with the following prompt to force the user to enter the Master Key or User hard disk drive password:

```
Enter Hard Disk Drive Password:
```

Upon successful entry of the Master Key or User hard disk drive password, the system will continue with normal POST.

If the hard disk drive password is not correctly entered, the system will go back to the above prompt. The user will have three attempts to correctly enter the hard disk drive password. After the third unsuccessful hard disk drive password attempt, the system will halt with the message:

```
Hard Disk Drive Password Entry Error
```

A manual power cycle will be required to resume system operation.

**NOTE**

*As implemented on DCP847SKE, Hard Disk Drive Password Security is only supported on SATA port 0. The passwords are stored on the hard disk drive so if the drive is relocated to another computer that does not support Hard Disk Drive Password Security feature, the drive will not be accessible.*

# 3.9 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is the user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.
- For enhanced security, use different passwords for the supervisor and user passwords.
- Valid password characters are A-Z, a-z, and 0-9. Passwords may be up to 16 characters in length.
- To clear a set password, enter a blank password after entering the existing password.

Table 25 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

**Table 25. Supervisor and User Password Functions**

| Password Set | Supervisor Mode | User Mode | Setup Options | Password to Enter Setup | Password During Boot |
|---|---|---|---|---|---|
| Neither | Can change all options (Note) | Can change all options (Note) | None | None | None |
| Supervisor only | Can change all options | Can change a limited number of options | Supervisor Password | Supervisor | None |
| User only | N/A | Can change all options | Enter Password<br>Clear User Password | User | User |
| Supervisor and user set | Can change all options | Can change a limited number of options | Supervisor Password<br>Enter Password | Supervisor or user | Supervisor or user |

Note: If no password is set, any user can change all Setup options.

# 4 Error Messages and Blink Codes

## 4.1 Front-panel Power LED Blink Codes

Whenever a recoverable error occurs during POST, the BIOS causes the board's front panel power LED to blink an error message describing the problem (see Table 26).

**Table 26. Front-panel Power LED Blink Codes**

| Type | Pattern | Note |
|---|---|---|
| BIOS update in progress | Off when the update begins, then on for 0.5 seconds, then off for 0.5 seconds. The pattern repeats until the BIOS update is complete. | |
| Video error (Note) | On-off (1.0 second each) two times, then 2.5-second pause (off), entire pattern repeats (blink and pause) until the system is powered off. | When no VGA option ROM is found. |
| Memory error | On-off (1.0 second each) three times, then 2.5-second pause (off), entire pattern repeats (blinks and pause) until the system is powered off. | |
| Thermal trip warning | Each beep will be accompanied by the following blink pattern: .25 seconds on, .25 seconds off, .25 seconds on, .25 seconds off. This will result in a total of 16 blinks. | |

Note: Disabled per default BIOS setup option.

## 4.2 BIOS Error Messages

Table 27 lists the error messages and provides a brief description of each.

**Table 27. BIOS Error Messages**

| Error Message | Explanation |
|---|---|
| CMOS Battery Low | The battery may be losing power. Replace the battery soon. |
| CMOS Checksum Bad | The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values. |
| Memory Size Decreased | Memory size has decreased since the last boot. If no memory was removed, then memory may be bad. |
| No Boot Device Available | System did not find a device to boot. |

# 4.3 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST codes requires a POST card that can interface with the Debug header. Refer to the location of the Debug header in Figure 1.

The following tables provide information about the POST codes generated by the BIOS:

- Table 28 lists the Port 80h POST code ranges
- Table 29 lists the Port 80h POST codes themselves
- Table 30 lists the Port 80h POST sequence

**NOTE**

*In the tables listed above, all POST codes and range values are listed in hexadecimal.*

**Table 28. Port 80h POST Code Ranges**

| Range | Subsystem |
|---|---|
| 0x00 – 0x05 | Entering SX states S0 to S5. |
| 0x10, 0x20, 0x30, 0x40, 0x50 | Resuming from SX states (0x10 –0x20 – S2, 0x30 – S3, etc.) |
| 0x01 – 0x0F | Security (SEC) phase |
| 0x11 – 0x1F | PEI phase pre MRC execution |
| 0x21 – 0x29 | MRC memory detection |
| 0x2A – 0x2F | PEI phase post MRC execution |
| 0x31 – 0x35 | Recovery |
| 0x36 – 0x3F | Platform DXE driver |
| 0x41 – 0x4F | CPU Initialization (PEI, DXE, SMM) |
| 0x50 – 0x5F | I/O Buses: PCI, USB, ATA etc. 0x5F is an unrecoverable error. Start with PCI. |
| 0x60 – 0x6F | BDS |
| 0x70 – 0x7F | Output devices: All output consoles. |
| 0x80 – 0x8F | For future use |
| 0x90 – 0x9F | Input devices: Keyboard/Mouse. |
| 0xA0 – 0xAF | For future use |
| 0xB0 – 0xBF | Boot Devices: Includes fixed media and removable media. Not that critical since consoles should be up at this point. |
| 0xC0 – 0xCF | For future use |
| 0xD0 – 0xDF | For future use |

**Table 29. Port 80h POST Codes**

| Port 80 Code | Progress Code Enumeration |
|---|---|
| | **ACPI S States** |
| 0x00,0x01,0x02,0x03,0x04,0x05 | Entering S0, S2, S3, S4, or S5 state |
| 0x10,0x20,0x30,0x40,0x50 | Resuming from S2, S3, S4, or S5 state |
| | **Security Phase (SEC)** |
| 0x08 | Starting BIOS execution after CPU BIST |
| 0x09 | SPI prefetching and caching |
| 0x0A | Load BSP microcode |
| 0x0B | Load APs microcode |
| 0x0C | Platform program baseaddresses |
| 0x0D | Wake Up All APs |
| 0x0E | Initialize NEM |
| 0x0F | Pass entry point of the PEI core |
| | **PEI before MRC** |
| | PEI Platform driver |
| 0x11 | Set bootmode, GPIO init |
| 0x12 | Early chipset register programming including graphics init |
| 0x13 | Basic PCH init, discrete device init (IEEE 1394, SATA) |
| 0x14 | LAN init |
| 0x15 | Exit early platform init driver |
| | **PEI SMBUS** |
| 0x16 | SMBUSriver init |
| 0x17 | Entry to SMBUS execute read/write |
| 0x18 | Exit SMBUS execute read/write |
| | **Memory** |
| 0x21 | MRC entry point |
| 0x22 | Reading SPD from memory DIMMs |
| 0x23 | Detecting presence of memory DIMMs |
| 0x25 | Configuring memory |
| 0x28 | Testing memory |
| 0x29 | Exit MRC driver |
| | **PEI after MRC** |
| 0x2A | Start to Program MTRR Settings |
| 0x2B | Done Programming MTRR Settings |

continued

**Table 29. Port 80h POST Codes** (continued)

| Port 80 Code | Progress Code Enumeration |
|---|---|
| | **PEIMs/Recovery** |
| 0x31 | Crisis Recovery has initiated |
| 0x34 | Loading recovery capsule |
| 0x35 | Start recovery capsule / valid capsule is found |
| | **CPU Initialization** |
| | **CPU PEI Phase** |
| 0x41 | Begin CPU PEI Init |
| 0x42 | XMM instruction enabling |
| 0x43 | End CPU PEI Init |
| | **CPU PEI SMM Phase** |
| 0x44 | Begin CPU SMM Init smm relocate bases |
| 0x45 | Smm relocate bases for APs |
| 0x46 | End CPU SMM Init |
| | **CPU DXE Phase** |
| 0x47 | CPU DXE Phase begin |
| 0x48 | Refresh memory space attributes according to MTRRs |
| 0x49 | Load the microcode if needed |
| 0x4A | Initialize strings to HII database |
| 0x4B | Initialize MP support |
| 0x4C | CPU DXE Phase End |
| | **CPU DXE SMM Phase** |
| 0x4D | CPU DXE SMM Phase begin |
| 0x4E | Relocate SM bases for all APs |
| 0x4F | CPU DXE SMM Phase end |
| | **I/O BUSES** |
| 0x50 | Enumerating PCI buses |
| 0x51 | Allocating resources to PCI bus |
| 0x52 | Hot Plug PCI controller initialization |
| | **USB** |
| 0x58 | Resetting USB bus |
| 0x59 | Reserved for USB |
| | **ATA/ATAPI/SATA** |
| 0x5A | Resetting PATA/SATA bus and all devices |
| 0x5B | Reserved for ATA |

continued

**Table 29. Port 80h POST Codes** (continued)

| Port 80 Code | Progress Code Enumeration |
|---|---|
| | **BDS** |
| 0x60 | BDS driver entry point initialize |
| 0x61 | BDS service routine entry point (can be called multiple times) |
| 0x62 | BDS Step2 |
| 0x63 | BDS Step3 |
| 0x64 | BDS Step4 |
| 0x65 | BDS Step5 |
| 0x66 | BDS Step6 |
| 0x67 | BDS Step7 |
| 0x68 | BDS Step8 |
| 0x69 | BDS Step9 |
| 0x6A | BDS Step10 |
| 0x6B | BDS Step11 |
| 0x6C | BDS Step12 |
| 0x6D | BDS Step13 |
| 0x6E | BDS Step14 |
| 0x6F | BDS return to DXE core (should not get here) |
| | **Keyboard (PS/2 or USB)** |
| 0x90 | Resetting keyboard |
| 0x91 | Disabling the keyboard |
| 0x92 | Detecting the presence of the keyboard |
| 0x93 | Enabling the keyboard |
| 0x94 | Clearing keyboard input buffer |
| 0x95 | Instructing keyboard controller to run Self Test (PS/2 only) |
| | **Mouse (PS/2 or USB)** |
| 0x98 | Resetting mouse |
| 0x99 | Detecting mouse |
| | Detecting presence of mouse |
| 0x9B | Enabling mouse |
| | **Fixed Media** |
| 0xB0 | Resetting fixed media |
| 0xB1 | Disabling fixed media |
| 0xB2 | Detecting presence of a fixed media (IDE hard drive detection etc.) |
| 0xB3 | Enabling/configuring a fixed media |

continued

**Table 29. Port 80h POST Codes** (continued)

| Port 80 Code | Progress Code Enumeration |
|---|---|
| | **Removable Media** |
| 0xB8 | Resetting removable media |
| 0xB9 | Disabling removable media |
| 0xBA | Detecting presence of a removable media (IDE, CDROM detection etc.) |
| 0xBC | Enabling/configuring a removable media |
| | **DXE Core** |
| 0xE4 | Entered DXE phase |
| | **BDS** |
| 0xE7 | Waiting for user input |
| 0xE8 | Checking password |
| 0xE9 | Entering BIOS setup |
| 0xEB | Calling Legacy Option ROMs |
| | **Runtime Phase/EFI OS Boot** |
| 0xF8 | EFI boot service ExitBootServices ( ) has been called |
| 0xF9 | EFI runtime service SetVirtualAddressMap ( ) has been called |

**Table 30. Typical Port 80h POST Sequence**

| POST Code | Description |
|---|---|
| 21 | Initializing a chipset component |
| 22 | Reading SPD from memory DIMMs |
| 23 | Detecting presence of memory DIMMs |
| 25 | Configuring memory |
| 28 | Testing memory |
| 34 | Loading recovery capsule |
| E4 | Entered DXE phase |
| 12 | Starting application processor initialization |
| 13 | SMM initialization |
| 50 | Enumerating PCI buses |
| 51 | Allocating resourced to PCI bus |
| 92 | Detecting the presence of the keyboard |
| 90 | Resetting keyboard |
| 94 | Clearing keyboard input buffer |
| 95 | Keyboard Self Test |
| EB | Calling Video BIOS |
| 58 | Resetting USB bus |
| 5A | Resetting PATA/SATA bus and all devices |
| 92 | Detecting the presence of the keyboard |
| 90 | Resetting keyboard |
| 94 | Clearing keyboard input buffer |
| 5A | Resetting PATA/SATA bus and all devices |
| 28 | Testing memory |
| 90 | Resetting keyboard |
| 94 | Clearing keyboard input buffer |
| E7 | Waiting for user input |
| 01 | INT 19 |
| 00 | Ready to boot |

# 5 Regulatory Compliance and Battery Disposal Information

## 5.1 Regulatory Compliance

This section contains the following regulatory compliance information for Intel Next Unit of Computing Board DCP847SKE:

- Safety standards
- European Union Declaration of Conformity statement
- Product Ecology statements
- Electromagnetic Compatibility (EMC) standards
- Product certification markings

### 5.1.1 Safety Standards

Intel Next Unit of Computing Board DCP847SKE complies with the safety standards stated in Table 31 when correctly installed in a compatible host system.

**Table 31. Safety Standards**

| Standard | Title |
|---|---|
| CSA/UL 60950-1 | Information Technology Equipment – Safety - Part 1: General Requirements (USA and Canada) |
| EN 60950-1 | Information Technology Equipment – Safety - Part 1: General Requirements (European Union) |
| IEC 60950-1 | Information Technology Equipment – Safety - Part 1: General Requirements (International) |

## 5.1.2 European Union Declaration of Conformity Statement

We, Intel Corporation, declare under our sole responsibility that the products Intel® Next Unit of Computing Board DCP847SKE is in conformity with all applicable essential requirements necessary for CE marking, following the provisions of the European Council Directive 2004/108/EC (EMC Directive), 2006/95/EC (Low Voltage Directive), and 2002/95/EC (ROHS Directive).

The product is properly CE marked demonstrating this conformity and is for distribution within all member states of the EU with no restrictions.

This product follows the provisions of the European Directives 2004/108/EC, 2006/95/EC, and 2002/95/EC.

***Čeština*** Tento výrobek odpovídá požadavkům evropských směrnic 2004/108/EC, 2006/95/EC a 2002/95/EC.

***Dansk*** Dette produkt er i overensstemmelse med det europæiske direktiv 2004/108/EC, 2006/95/EC & 2002/95/EC.

***Dutch*** Dit product is in navolging van de bepalingen van Europees Directief 2004/108/EC, 2006/95/EC & 2002/95/EC.

***Eesti*** Antud toode vastab Euroopa direktiivides 2004/108/EC, ja 2006/95/EC ja 2002/95/EC kehtestatud nõuetele.

***Suomi*** Tämä tuote noudattaa EU-direktiivin 2004/108/EC, 2006/95/EC & 2002/95/EC määräyksiä.

***Français*** Ce produit est conforme aux exigences de la Directive Européenne 2004/108/EC, 2006/95/EC & 2002/95/EC.

***Deutsch*** Dieses Produkt entspricht den Bestimmungen der Europäischen Richtlinie 2004/108/EC, 2006/95/EC & 2002/95/EC.

**Ελληνικά** Το παρόν προϊόν ακολουθεί τις διατάξεις των Ευρωπαϊκών Οδηγιών 2004/108/EC, 2006/95/EC και 2002/95/EC.

***Magyar*** E termék megfelel a 2004/108/EC, 2006/95/EC és 2002/95/EC Európai Irányelv előírásainak.

***Icelandic*** Þessi vara stenst reglugerð Evrópska Efnahags Bandalagsins númer 2004/108/EC, 2006/95/EC, & 2002/95/EC.

***Italiano*** Questo prodotto è conforme alla Direttiva Europea 2004/108/EC, 2006/95/EC & 2002/95/EC.

***Latviešu*** Šis produkts atbilst Eiropas Direktīvu 2004/108/EC, 2006/95/EC un 2002/95/EC noteikumiem.

***Lietuvių*** Šis produktas atitinka Europos direktyvų 2004/108/EC, 2006/95/EC, ir 2002/95/EC nuostatas.

***Malti*** Dan il-prodott hu konformi mal-provvedimenti tad-Direttivi Ewropej 2004/108/EC, 2006/95/EC u 2002/95/EC.

***Norsk*** Dette produktet er i henhold til bestemmelsene i det europeiske direktivet 2004/108/EC, 2006/95/EC & 2002/95/EC.

***Polski*** Niniejszy produkt jest zgodny z postanowieniami Dyrektyw Unii Europejskiej 2004/108/EC, 206/95/EC i 2002/95/EC.

***Portuguese*** Este produto cumpre com as normas da Diretiva Européia 2004/108/EC, 2006/95/EC & 2002/95/EC.

***Español*** Este producto cumple con las normas del Directivo Europeo 2004/108/EC, 2006/95/EC & 2002/95/EC.

***Slovensky*** Tento produkt je v súlade s ustanoveniami európskych direktív 2004/108/EC, 2006/95/EC a 2002/95/EC.

***Slovenščina*** Izdelek je skladen z določbami evropskih direktiv 2004/108/EC, 2006/95/EC in 2002/95/EC.

***Svenska*** Denna produkt har tillverkats i enlighet med EG-direktiv 2004/108/EC, 2006/95/EC & 2002/95/EC.

***Türkçe*** Bu ürün, Avrupa Birliği'nin 2004/108/EC, 2006/95/EC ve 2002/95/EC yönergelerine uyar.

## 5.1.3 Product Ecology Statements

The following information is provided to address worldwide product ecology concerns and regulations.

### 5.1.3.1 Disposal Considerations

This product contains the following materials that may be regulated upon disposal: lead solder on the printed wiring board assembly.

### 5.1.3.2 Recycling Considerations

As part of its commitment to environmental responsibility, Intel has implemented the Intel Product Recycling Program to allow retail consumers of Intel's branded products to return used products to selected locations for proper recycling.

Please consult the http://www.intel.com/intel/other/ehs/product_ecology for the details of this program, including the scope of covered products, available locations, shipping instructions, terms and conditions, etc.

**中文**

作为其对环境责任之承诺的部分，英特尔已实施 Intel Product Recycling Program（英特尔产品回收计划），以允许英特尔品牌产品的零售消费者将使用过的产品退还至指定地点作恰当的重复使用处理。

请参考http://www.intel.com/intel/other/ehs/product_ecology 了解此计划的详情，包括涉及产品之范围、回收地点、运送指导、条款和条件等。

***Deutsch***

Als Teil von Intels Engagement für den Umweltschutz hat das Unternehmen das Intel Produkt-Recyclingprogramm implementiert, das Einzelhandelskunden von Intel Markenprodukten ermöglicht, gebrauchte Produkte an ausgewählte Standorte für ordnungsgemäßes Recycling zurückzugeben.

Details zu diesem Programm, einschließlich der darin eingeschlossenen Produkte, verfügbaren Standorte, Versandanweisungen, Bedingungen usw., finden Sie auf der http://www.intel.com/intel/other/ehs/product_ecology

***Español***

Como parte de su compromiso de responsabilidad medioambiental, Intel ha implantado el programa de reciclaje de productos Intel, que permite que los consumidores al detalle de los productos Intel devuelvan los productos usados en los lugares seleccionados para su correspondiente reciclado.

Consulte la http://www.intel.com/intel/other/ehs/product_ecology para ver los detalles del programa, que incluye los productos que abarca, los lugares disponibles, instrucciones de envío, términos y condiciones, etc.

***Français***

Dans le cadre de son engagement pour la protection de l'environnement, Intel a mis en œuvre le programme Intel Product Recycling Program (Programme de recyclage des produits Intel) pour permettre aux consommateurs de produits Intel de recycler les produits usés en les retournant à des adresses spécifiées.

Visitez la page Web http://www.intel.com/intel/other/ehs/product_ecology pour en savoir plus sur ce programme, à savoir les produits concernés, les adresses disponibles, les instructions d'expédition, les conditions générales, etc.

日本語

インテルでは、環境保護活動の一環として、使い終えたインテル
ブランド製品を指定の場所へ返送していただき、リサイクルを適切に行えるよう、インテル製品リサイクル
プログラムを発足させました。

対象製品、返送先、返送方法、ご利用規約など、このプログラムの詳細情報は、http://www.intel.com/intel/other/ehs/product_ecology（英語）をご覧ください。

***Malay***

Sebagai sebahagian daripada komitmennya terhadap tanggungjawab persekitaran, Intel telah melaksanakan Program Kitar Semula Produk untuk membenarkan pengguna-pengguna runcit produk jenama Intel memulangkan produk terguna ke lokasi-lokasi terpilih untuk dikitarkan semula dengan betul.

Sila rujuk http://www.intel.com/intel/other/ehs/product_ecology untuk mendapatkan butir-butir program ini, termasuklah skop produk yang dirangkumi, lokasi-lokasi tersedia, arahan penghantaran, terma & syarat, dsb.

***Portuguese***

Como parte deste compromisso com o respeito ao ambiente, a Intel implementou o Programa de Reciclagem de Produtos para que os consumidores finais possam enviar produtos Intel usados para locais selecionados, onde esses produtos são reciclados de maneira adequada.

Consulte o site http://www.intel.com/intel/other/ehs/product_ecology (em Inglês) para obter os detalhes sobre este programa, inclusive o escopo dos produtos cobertos, os locais disponíveis, as instruções de envio, os termos e condições, etc.

***Russian***

В качестве части своих обязательств к окружающей среде, в Intel создана программа утилизации продукции Intel (Product Recycling Program) для предоставления конечным пользователям марок продукции Intel возможности возврата используемой продукции в специализированные пункты для должной утилизации.

Пожалуйста, обратитесь на веб-сайт http://www.intel.com/intel/other/ehs/product_ecology за информацией об этой программе, принимаемых продуктах, местах приема, инструкциях об отправке, положениях и условиях и т.д.

***Türkçe***

Intel, çevre sorumluluğuna bağımlılığının bir parçası olarak, perakende tüketicilerin Intel markalı kullanılmış ürünlerini belirlenmiş merkezlere iade edip uygun şekilde geri dönüştürmesini amaçlayan Intel Ürünleri Geri Dönüşüm Programı'nı uygulamaya koymuştur.

Bu programın ürün kapsamı, ürün iade merkezleri, nakliye talimatları, kayıtlar ve şartlar v.s dahil bütün ayrıntılarını ögrenmek için lütfen http://www.intel.com/intel/other/ehs/product_ecology

Web sayfasına gidin.

### 5.1.4 EMC Regulations

Intel Next Unit of Computing Board DCP847SKE complies with the EMC regulations stated in Table 32 when correctly installed in a compatible host system.

**Table 32. EMC Regulations**

| Regulation | Title |
|---|---|
| FCC 47 CFR Part 15, Subpart B | Title 47 of the Code of Federal Regulations, Part 15, Subpart B, Radio Frequency Devices. (USA) |
| ICES-003 | Interference-Causing Equipment Standard, Digital Apparatus. (Canada) |
| EN55022 | Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (European Union) |
| EN55024 | Information Technology Equipment – Immunity Characteristics Limits and methods of measurement. (European Union) |
| EN55022 | Australian Communications Authority, Standard for Electromagnetic Compatibility. (Australia and New Zealand) |
| CISPR 22 | Limits and methods of measurement of Radio Disturbance Characteristics of Information Technology Equipment. (International) |
| CISPR 24 | Information Technology Equipment – Immunity Characteristics – Limits and Methods of Measurement. (International) |
| VCCI V-3, V-4 | Voluntary Control for Interference by Information Technology Equipment. (Japan) |
| KN-22, KN-24 | Korean Communications Commission – Framework Act on Telecommunications and Radio Waves Act (South Korea) |
| CNS 13438 | Bureau of Standards, Metrology, and Inspection (Taiwan) |

### FCC Declaration of Conformity

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

For questions related to the EMC performance of this product, contact:

Intel Corporation, 5200 N.E. Elam Young Parkway, Hillsboro, OR 97124
1-800-628-8686

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment to an outlet on a circuit other than the one to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications to the equipment not expressly approved by Intel Corporation could void the user's authority to operate the equipment.

Tested to comply with FCC standards for home or office use.

### Canadian Department of Communications Compliance Statement

This digital apparatus does not exceed the Class B limits for radio noise emissions from digital apparatus set out in the Radio Interference Regulations of the Canadian Department of Communications.

Le présent appareil numerique német pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de la classe B prescrites dans le Réglement sur le broullage radioélectrique édicté par le ministére des Communications du Canada.

### Japan VCCI Statement

Japan VCCI Statement translation: This is a Class B product based on the standard of the Voluntary Control Council for Interference from Information Technology Equipment (VCCI). If this is used near a radio or television receiver in a domestic environment, it may cause radio interference. Install and use the equipment according to the instruction manual.

この装置は、情報処理装置等電波障害自主規制協議会（ＶＣＣＩ）の基準に基づくクラスＢ情報技術装置です。この装置は、家庭環境で使用することを目的としていますが、この装置がラジオやテレビジョン受信機に近接して使用されると、受信障害を引き起こすことがあります。
取扱説明書に従って正しい取り扱いをして下さい。

### Korea Class B Statement

Korea Class B Statement translation: This equipment is for home use, and has acquired electromagnetic conformity registration, so it can be used not only in residential areas, but also other areas.

이 기기는 가정용(B급) 전자파적합기기로서 주 로 가정에서 사용하는 것을 목적으로 하며, 모 든 지역에서 사용할 수 있습니다.

### 5.1.5 ENERGY STAR* 5.2, e-Standby, and ErP Compliance

The US Department of Energy and the US Environmental Protection Agency have continually revised the ENERGY STAR requirements. Intel has worked directly with these two governmental agencies in the definition of new requirements.

Intel Next Unit of Computing Board DCP847SKE meets the following program requirements in an adequate system configuration, including appropriate selection of an efficient power supply:

- Energy Star v5.2, category B
- EPEAT*
- Korea e-Standby
- European Union Energy-related Products Directive 2013 (ErP) Lot 6

**NOTE**

*Energy Star compliance is based at the system level not the board level. Use of an Intel Next Unit of Computing Board alone does not guarantee Energy Star compliance.*

| For information about | Refer to |
|---|---|
| ENERGY STAR requirements and recommended configurations | http://www.intel.com/go/energystar |
| Electronic Product Environmental Assessment Tool (EPEAT) | http://www.epeat.net/ |
| Korea e-Standby Program | http://www.kemco.or.kr/new_eng/pg02/pg02100300.asp |
| European Union Energy-related Products Directive 2009 (ErP) | http://ec.europa.eu/enterprise/policies/sustainable-business/sustainable-product-policy/ecodesign/index_en.htm |

### 5.1.6 Regulatory Compliance Marks (Board Level)

Intel Next Unit of Computing Board DCP847SKE has the regulatory compliance marks shown in Table 33.

**Table 33. Regulatory Compliance Marks**

| Description | Mark |
|---|---|
| UL joint US/Canada Recognized Component mark. Includes adjacent UL file number for Intel Next Unit of Computing Boards: E210882. |  |
| FCC Declaration of Conformity logo mark for Class B equipment. |  |
| CE mark. Declaring compliance to the European Union (EU) EMC directive, Low Voltage directive, and RoHS directive. |  |
| Australian Communications Authority (ACA) and New Zealand Radio Spectrum Management (NZ RSM) C-tick mark. Includes adjacent Intel supplier code number, N-232. |  |
| Japan VCCI (Voluntary Control Council for Interference) mark. |  |
| Korea Certification mark. Includes an adjacent KCC (Korean Communications Commission) certification number: KCC-REM-CPU-DCP847SKE. |  |
| Taiwan BSMI (Bureau of Standards, Metrology and Inspections) mark. Includes adjacent Intel company number, D33025. |  |
| Printed wiring board manufacturer's recognition mark. Consists of a unique UL recognized manufacturer's logo, along with a flammability rating (solder side). | V-0 |
| China RoHS/Environmentally Friendly Use Period Logo: This is an example of the symbol used on Intel Next Unit of Computing Boards and associated collateral. The color of the mark may vary depending upon the application. The Environmental Friendly Usage Period (EFUP) for Intel Next Unit of Computing Boards has been determined to be 10 years. |  |

## 5.2 Battery Disposal Information

**CAUTION**

*Risk of explosion if the battery is replaced with an incorrect type. Batteries should be recycled where possible. Disposal of used batteries must be in accordance with local environmental regulations.*

PRÉCAUTION

*Risque d'explosion si la pile usagée est remplacée par une pile de type incorrect. Les piles usagées doivent être recyclées dans la mesure du possible. La mise au rebut des piles usagées doit respecter les réglementations locales en vigueur en matière de protection de l'environnement.*

FORHOLDSREGEL

*Eksplosionsfare, hvis batteriet erstattes med et batteri af en forkert type. Batterier bør om muligt genbruges. Bortskaffelse af brugte batterier bør foregå i overensstemmelse med gældende miljølovgivning.*

OBS!

*Det kan oppstå eksplosjonsfare hvis batteriet skiftes ut med feil type. Brukte batterier bør kastes i henhold til gjeldende miljølovgivning.*

VIKTIGT!

*Risk för explosion om batteriet ersätts med felaktig batterityp. Batterier ska kasseras enligt de lokala miljövårdsbestämmelserna.*

VARO

*Räjähdysvaara, jos pariston tyyppi on väärä. Paristot on kierrätettävä, jos se on mahdollista. Käytetyt paristot on hävitettävä paikallisten ympäristömääräysten mukaisesti.*

VORSICHT

*Bei falschem Einsetzen einer neuen Batterie besteht Explosionsgefahr. Die Batterie darf nur durch denselben oder einen entsprechenden, vom Hersteller empfohlenen Batterietyp ersetzt werden. Entsorgen Sie verbrauchte Batterien den Anweisungen des Herstellers entsprechend.*

AVVERTIMENTO

*Esiste il pericolo di un esplosione se la pila non viene sostituita in modo corretto. Utilizzare solo pile uguali o di tipo equivalente a quelle consigliate dal produttore. Per disfarsi delle pile usate, seguire le istruzioni del produttore.*

## PRECAUCIÓN

*Existe peligro de explosión si la pila no se cambia de forma adecuada. Utilice solamente pilas iguales o del mismo tipo que las recomendadas por el fabricante del equipo. Para deshacerse de las pilas usadas, siga igualmente las instrucciones del fabricante.*

## WAARSCHUWING

*Er bestaat ontploffingsgevaar als de batterij wordt vervangen door een onjuist type batterij. Batterijen moeten zoveel mogelijk worden gerecycled. Houd u bij het weggooien van gebruikte batterijen aan de plaatselijke milieuwetgeving.*

## ATENÇÃO

*Haverá risco de explosão se a bateria for substituída por um tipo de bateria incorreto. As baterias devem ser recicladas nos locais apropriados. A eliminação de baterias usadas deve ser feita de acordo com as regulamentações ambientais da região.*

## AŚCIAROŽZNAŚĆ

*Існуе рызыка выбуху, калі заменены акумулятар неправільнага тыпу. Акумулятары павінны, па магчымасці, перепрацоўвацца. Пазбаўляцца ад старых акумулятараў патрэбна згодна з мясцовым заканадаўствам па экалогіі.*

## UPOZORNÌNÍ

*V případě výměny baterie za nesprávný druh může dojít k výbuchu. Je-li to možné, baterie by měly být recyklovány. Baterie je třeba zlikvidovat v souladu s místními předpisy o životním prostředí.*

## Προσοχή

*Υπάρχει κίνδυνος για έκρηξη σε περίπτωση που η μπαταρία αντικατασταθεί από μία λανθασμένου τύπου. Οι μπαταρίες θα πρέπει να ανακυκλώνονται όταν κάτι τέτοιο είναι δυνατό. Η απόρριψη των χρησιμοποιημένων μπαταριών πρέπει να γίνεται σύμφωνα με τους κατά τόπο περιβαλλοντικούς κανονισμούς.*

## VIGYÁZAT

*Ha a telepet nem a megfelelő típusú telepre cseréli, az felrobbanhat. A telepeket lehetőség szerint újra kell hasznosítani. A használt telepeket a helyi környezetvédelmi előírásoknak megfelelően kell kiselejtezni.*

## 注意

異なる種類の電池を使用すると、爆発の危険があります。リサイクルが可能な地域であれば、電池をリサイクルしてください。使用後の電池を廃棄する際には、地域の環境規制に従ってください。

AWAS

*Risiko letupan wujud jika bateri digantikan dengan jenis yang tidak betul. Bateri sepatutnya dikitar semula jika boleh. Pelupusan bateri terpakai mestilah mematuhi peraturan alam sekitar tempatan.*

OSTRZEŻENIE

*Istnieje niebezpieczeństwo wybuchu w przypadku zastosowania niewłaściwego typu baterii. Zużyte baterie należy w miarę możliwości utylizować zgodnie z odpowiednimi przepisami ochrony środowiska.*

PRECAUȚIE

*Risc de explozie, dacă bateria este înlocuită cu un tip de baterie necorespunzător. Bateriile trebuie reciclate, dacă este posibil. Depozitarea bateriilor uzate trebuie să respecte reglementările locale privind protecţia mediului.*

ВНИМАНИЕ

*При использовании батареи несоответствующего типа существует риск ее взрыва. Батареи должны быть утилизированы по возможности. Утилизация батарей должна проводится по правилам, соответствующим местным требованиям.*

UPOZORNENIE

*Ak batériu vymeníte za nesprávny typ, hrozí nebezpečenstvo jej výbuchu.*
*Batérie by sa mali podľa možnosti vždy recyklovať. Likvidácia použitých batérií sa musí vykonávať v súlade s miestnymi predpismi na ochranu životného prostredia.*

POZOR

*Zamenjava baterije z baterijo drugačnega tipa lahko povzroči eksplozijo.*
*Če je mogoče, baterije reciklirajte. Rabljene baterije zavrzite v skladu z lokalnimi okoljevarstvenimi predpisi.*

***คำเตือน***

***ระวังการระเบิดที่เกิดจากเปลี่ยนแบตเตอรี่ผิดประเภท หากเป็นไปได้ ควรนำแบตเตอรี่ไปรีไซเคิล การทิ้งแบตเตอรี่ใช้แล้วต้องเป็นไปตามกฎข้อบังคับด้านสิ่งแวดล้อมของท้องถิ่น.***

UYARI

*Yanlış türde pil takıldığında patlama riski vardır. Piller mümkün olduğunda geri dönüştürülmelidir. Kullanılmış piller, yerel çevre yasalarına uygun olarak atılmalıdır.*

ОСТОРОГА

*Використовуйте батареї правильного типу, інакше існуватиме ризик вибуху. Якщо можливо, використані батареї слід утилізувати. Утилізація використаних батарей має бути виконана згідно місцевих норм, що регулюють охорону довкілля.*

## UPOZORNĚNÍ

*V případě výměny baterie za nesprávný druh může dojít k výbuchu. Je-li to možné, baterie by měly být recyklovány. Baterie je třeba zlikvidovat v souladu s místními předpisy o životním prostředí.*

## ETTEVAATUST

*Kui patarei asendatakse uue ebasobivat tüüpi patareiga, võib tekkida plahvatusoht. Tühjad patareid tuleb võimaluse korral viia vastavasse kogumispunkti. Tühjade patareide äraviskamisel tuleb järgida kohalikke keskkonnakaitse alaseid reegleid.*

## FIGYELMEZTETÉS

*Ha az elemet nem a megfelelő típusúra cseréli, felrobbanhat. Az elemeket lehetőség szerint újra kell hasznosítani. A használt elemeket a helyi környezetvédelmi előírásoknak megfelelően kell kiselejtezni.*

## UZMANĪBU

*Pastāv eksplozijas risks, ja baterijas tiek nomainītas ar nepareiza veida baterijām. Ja iespējams, baterijas vajadzētu nodot attiecīgos pieņemšanas punktos. Bateriju izmešanai atkritumos jānotiek saskaņā ar vietējiem vides aizsardzības noteikumiem.*

## DĖMESIO

*Naudojant netinkamo tipo baterijas įrenginys gali sprogti. Kai tik įmanoma, baterijas reikia naudoti pakartotinai. Panaudotas baterijas išmesti būtina pagal vietinius aplinkos apsaugos nuostatus.*

## ATTENZJONI

*Riskju ta' splużjoni jekk il-batterija tinbidel b'tip ta' batterija mhux korrett. Il-batteriji għandhom jiġu riċiklati fejn hu possibbli. Ir-rimi ta' batteriji użati għandu jsir skond ir-regolamenti ambjentali lokali.*

## OSTRZEŻENIE

*Ryzyko wybuchu w przypadku wymiany na baterie niewłaściwego typu. W miarę możliwości baterie należy poddać recyklingowi. Zużytych baterii należy pozbywać się zgodnie z lokalnie obowiązującymi przepisami w zakresie ochrony środowiska.*